

# Compal Confidential

## QIWG7 DIS M/B Schematics Document

### Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

### nVIDIA N13P-GL

2011-12-28

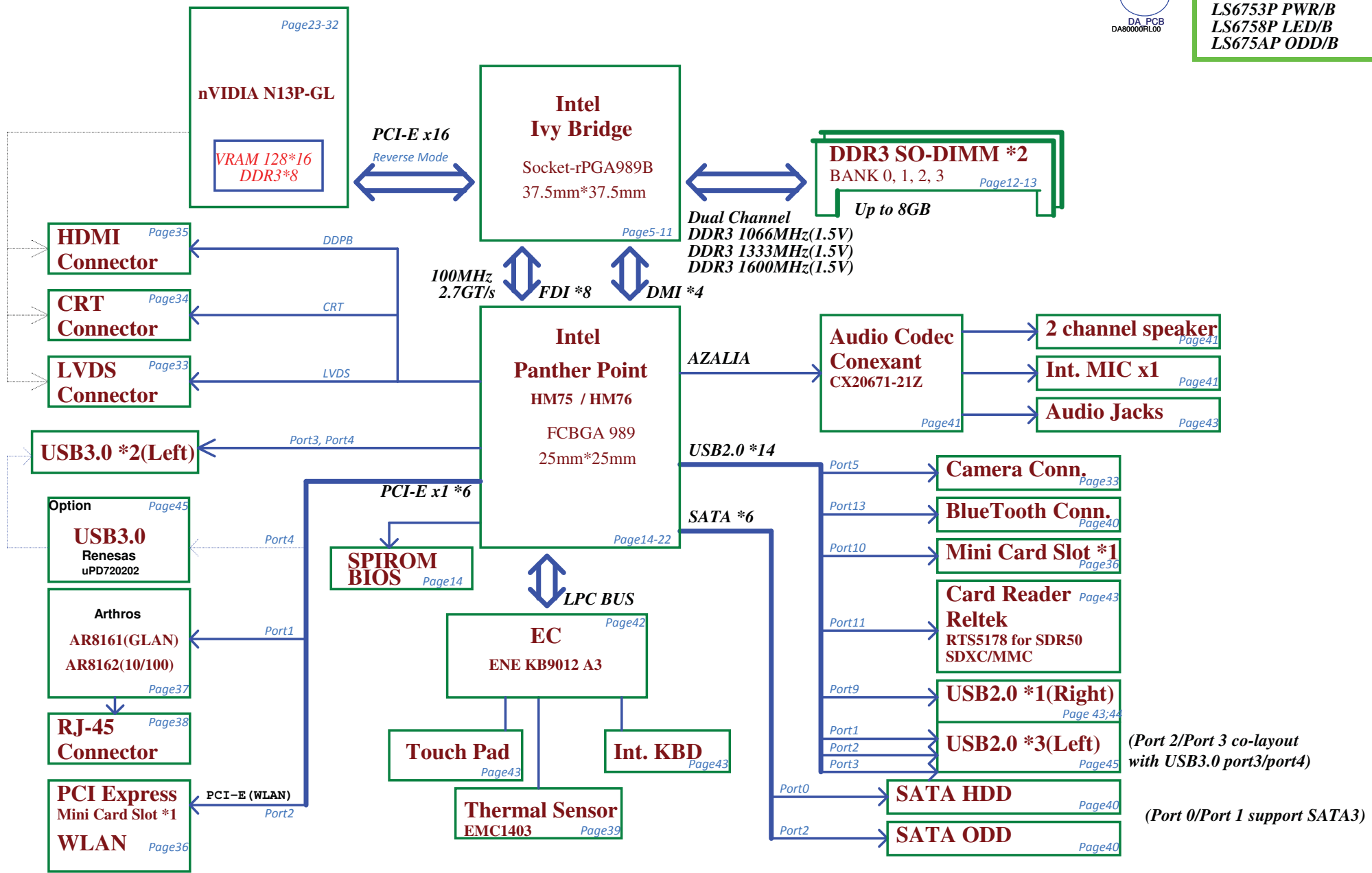
LA-7983P

REV: 0.3

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
				Cover Page	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
Date: Thursday, January 05, 2012				Sheet	1 of 60



LS7988P CR\_AUDIO/B  
LS7987P USB/B  
LS6753P PWR/B  
LS6758P LED/B  
LS675AP ODD/B



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Block Diagram
Date: Thursday, January 05, 2012				Rev 0.3

## Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG
				+1.8VS +0.75VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor F75030M	1001_101xb

## PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

## NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

## USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0
		1
	UHCI1	2
		3
	UHCI2	4
		5
	UHCI3	6
EHCI2		7
	UHCI4	8
		9
	UHCI5	10
		11
	UHCI6	12
		13

## BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
UMA only	UMA@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
Camera	CMOS@
Green Clock	GCLK@
	GCLK244@
Unpop	@

## SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	✗	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

Security Classification	Compal Secret Data				Compal Electronics, Inc.			
Issued Date	2011/10/27	Deciphered Date	2012/10/27		Title	Notes List		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Document Number	LA-7983P	Rev	0.3
					Date	Thursday, January 05, 2012	Sheet	3 of 60

Hot plug detect for IFP link C

## VGA and GDDR3 Voltage Rails (N13P GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

## Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

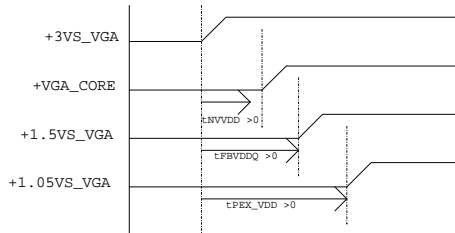
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

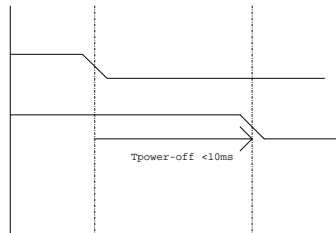
	Device ID
N13P-GL (28nm)	???

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL	Samsung 900MHz						
		64Mx16	PD 10K PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz	64Mx16	PD 10K PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
		128Mx16	PD 10K PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz	128Mx16	PD 10K PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

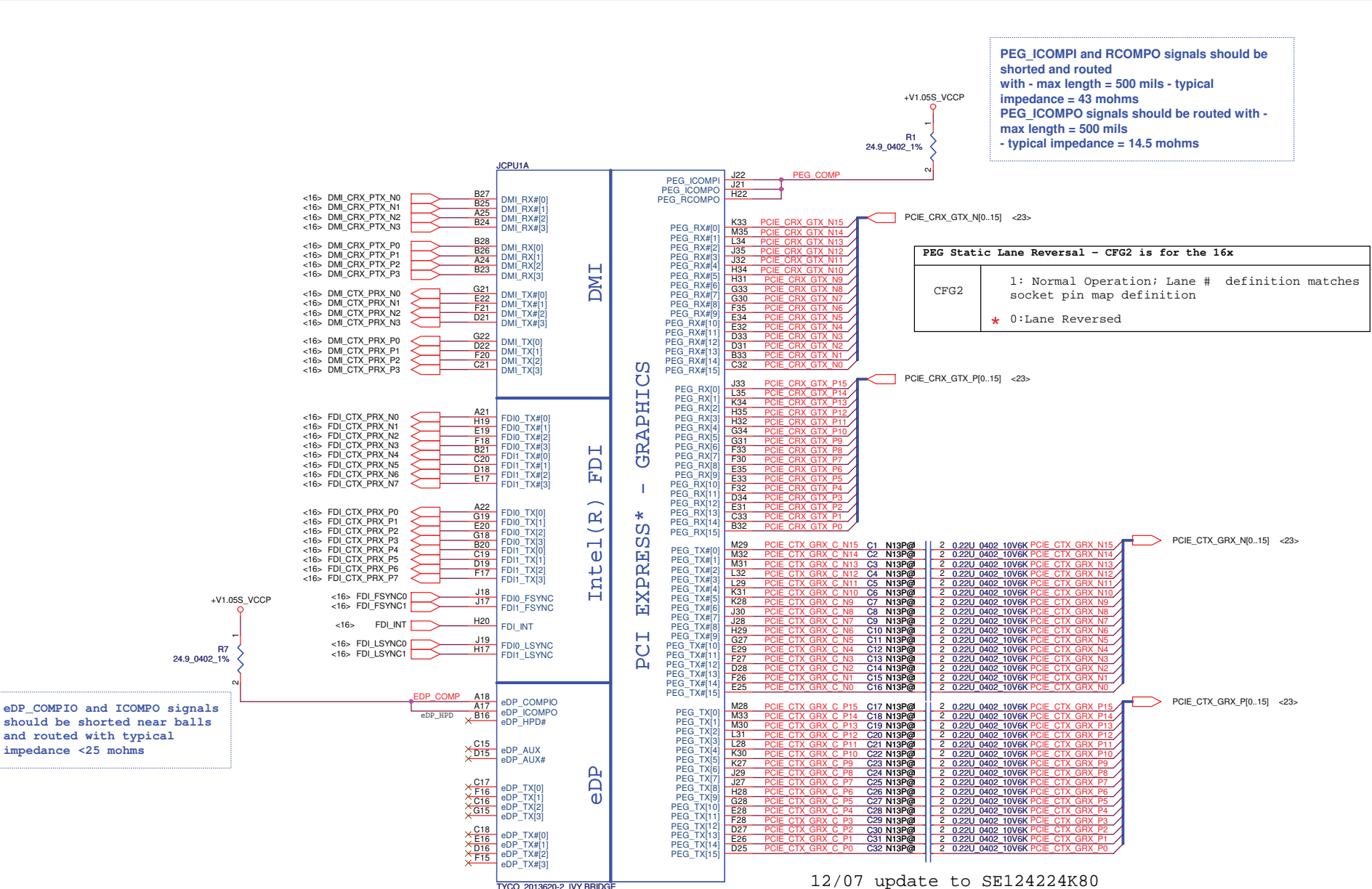


- all power rail ramp up time should be larger than 40us
- Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



- all GPU power rails should be turned off within 10ms

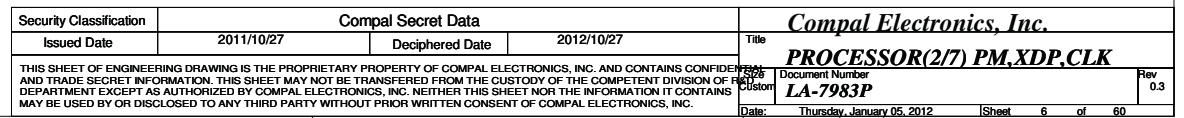
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	VGA Notes List
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-7983P	Rev 0.3
				Date Thursday, January 05, 2012	Sheet 4 of 60

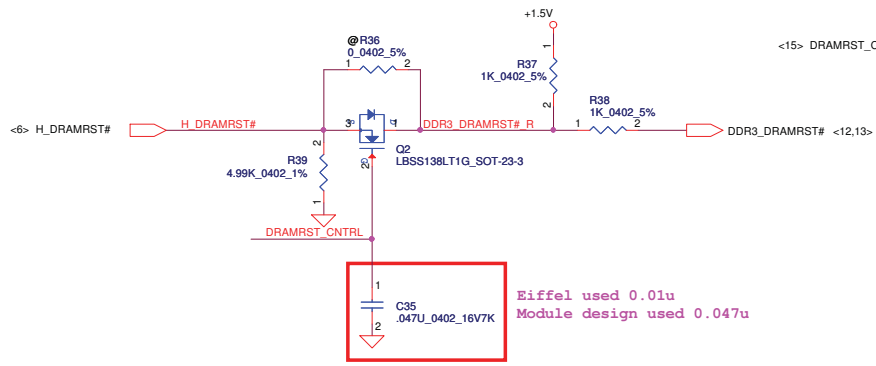
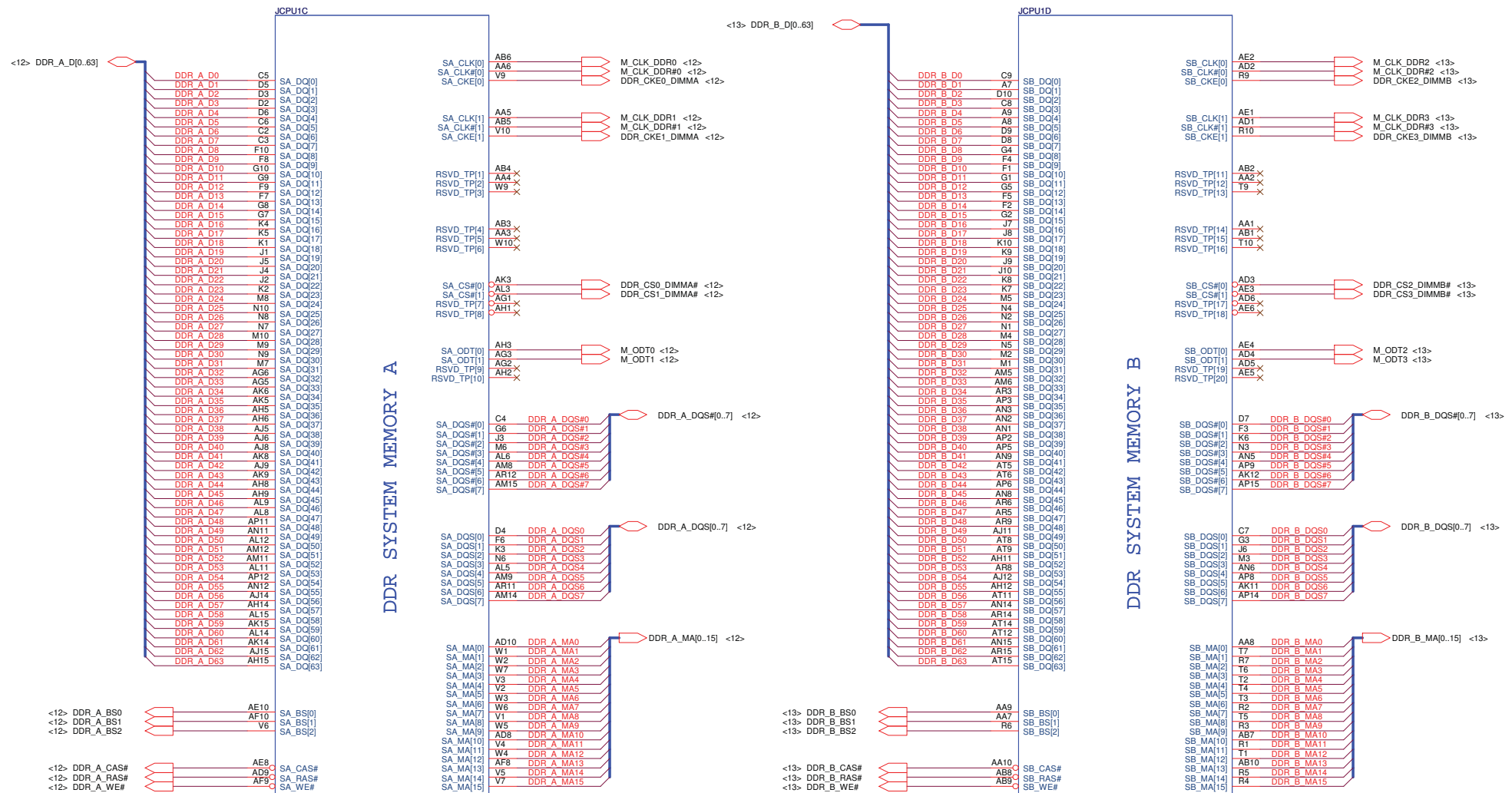


PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

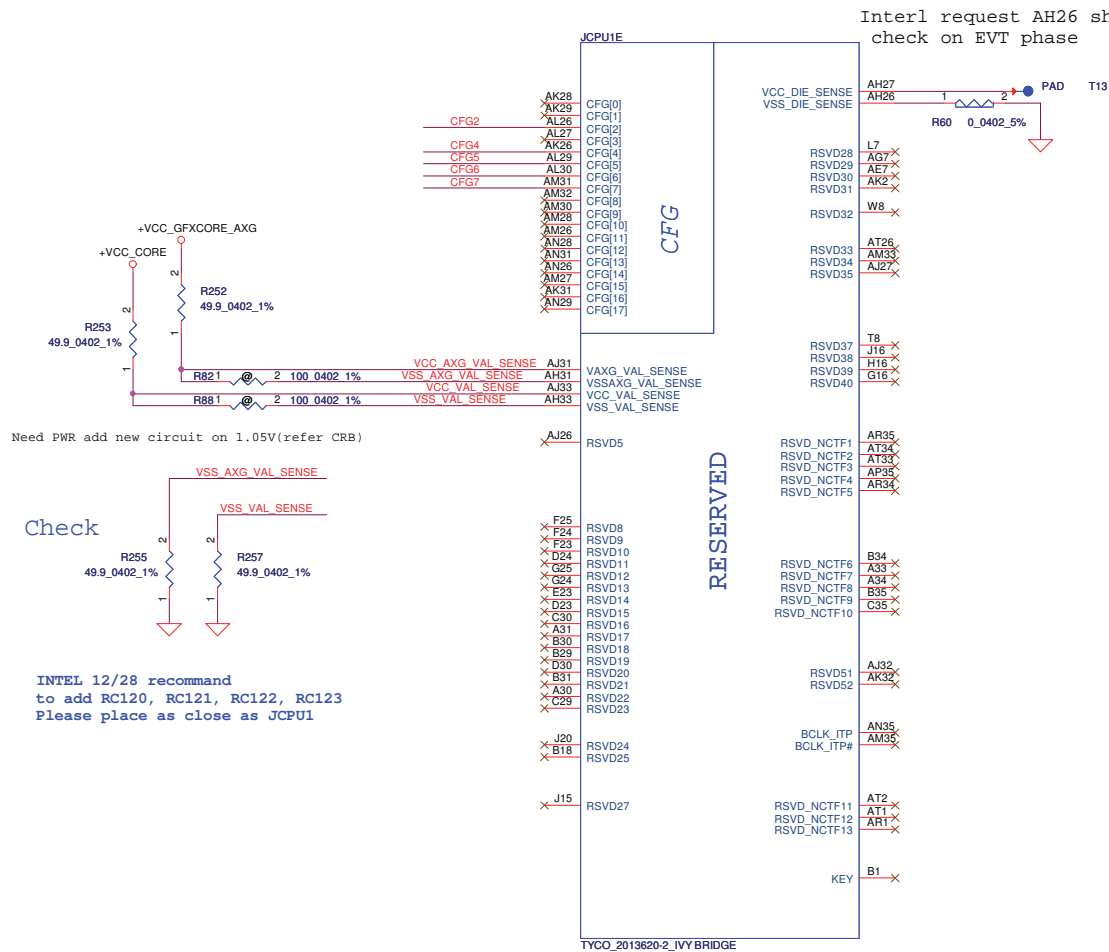
12/07 update to SE124224K80





Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2011/10/27	
2011/10/27		2012/10/27		Rev	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number		Rev	
LA-7983P		Thursday, January 05, 2012		Sheet 7 of 60	
Date		Sheet		of	
7		60		0.3	

## CFG Straps for Processor



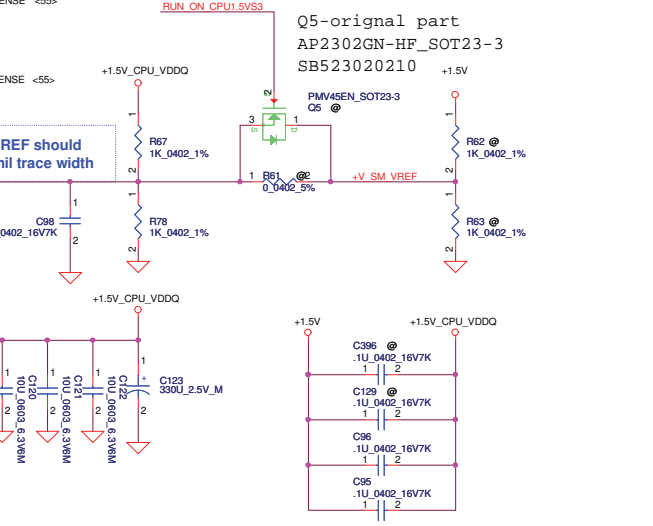
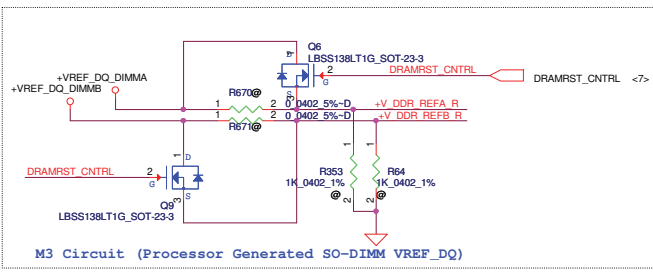
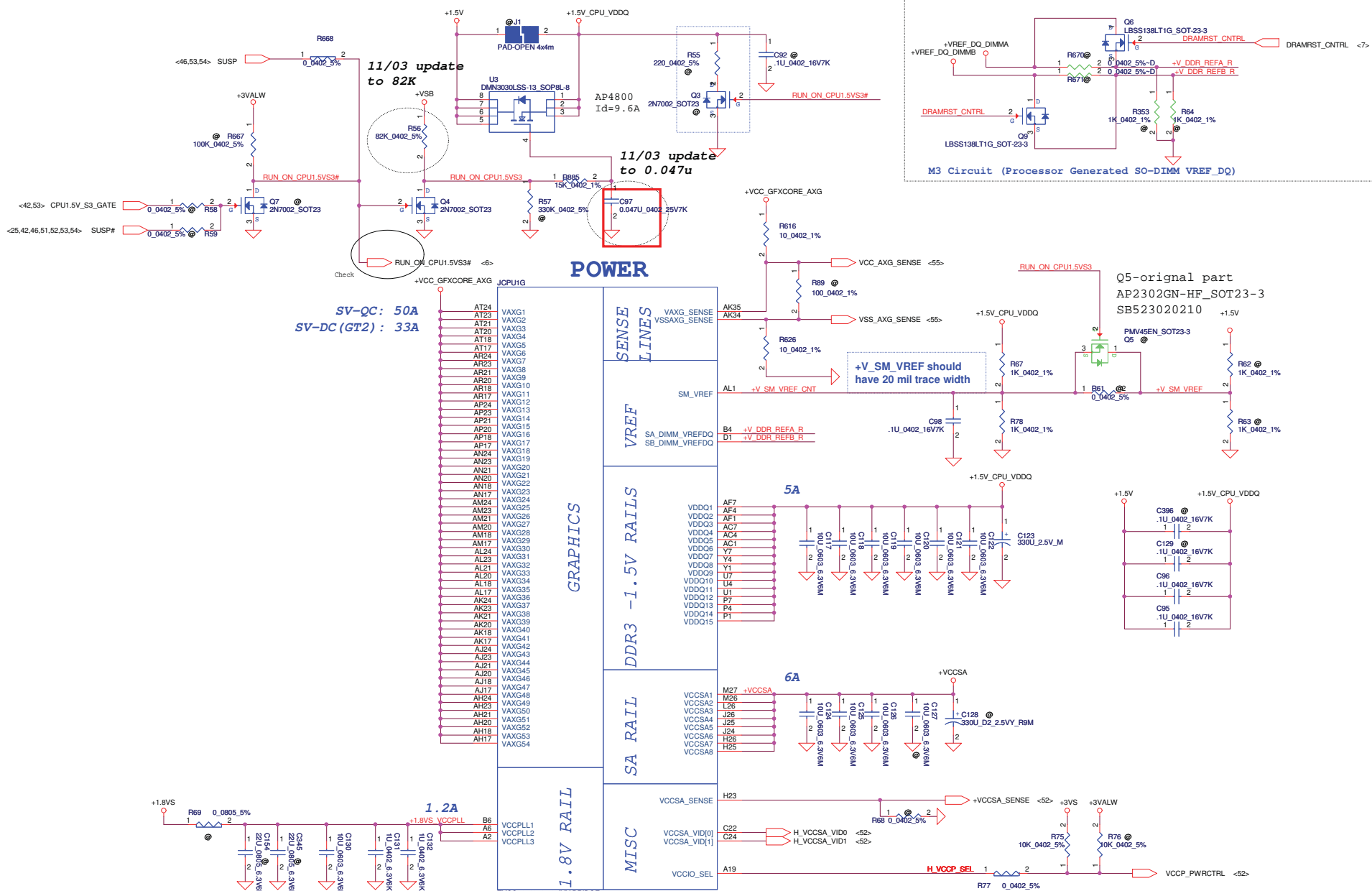
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

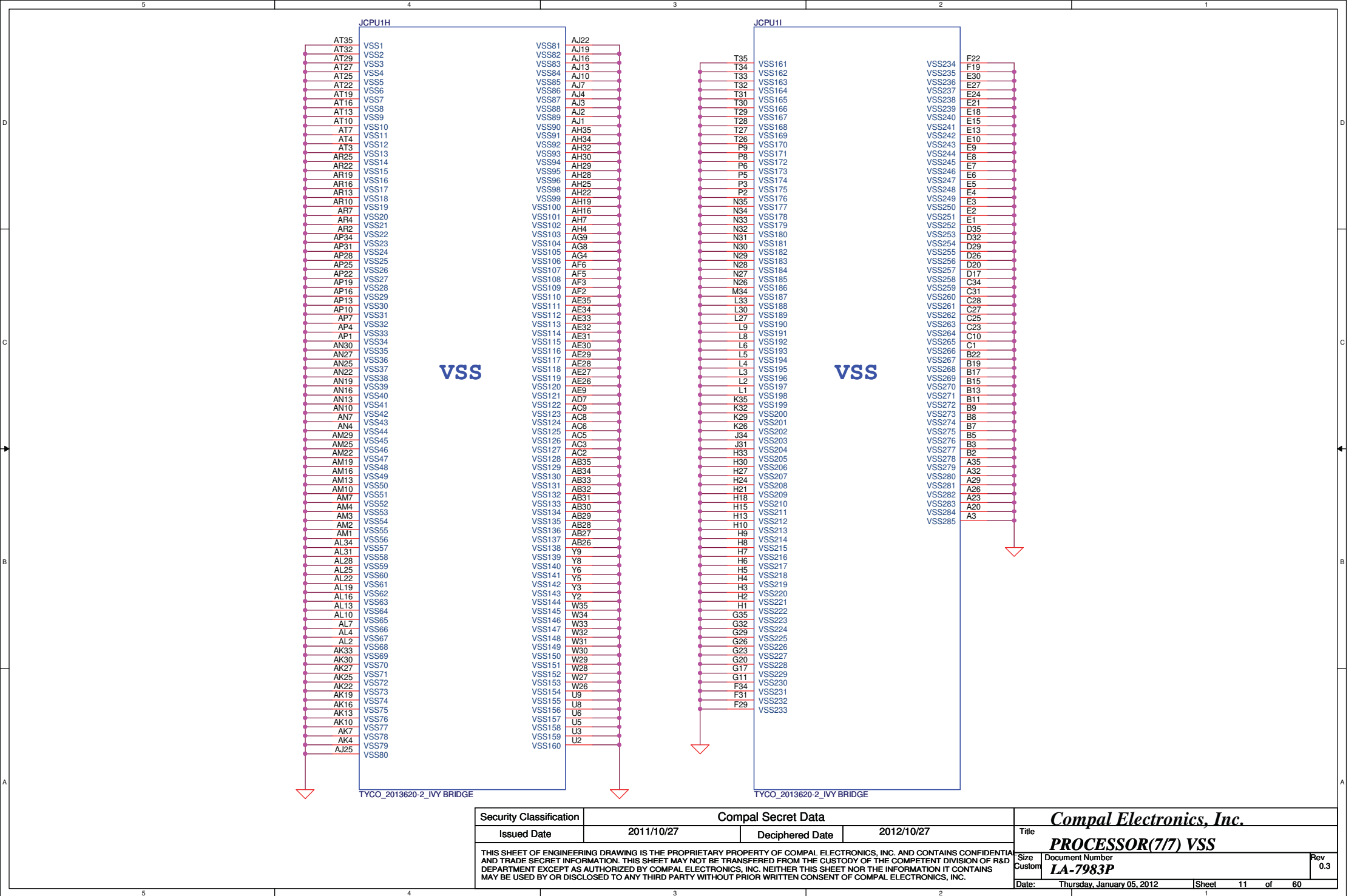
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





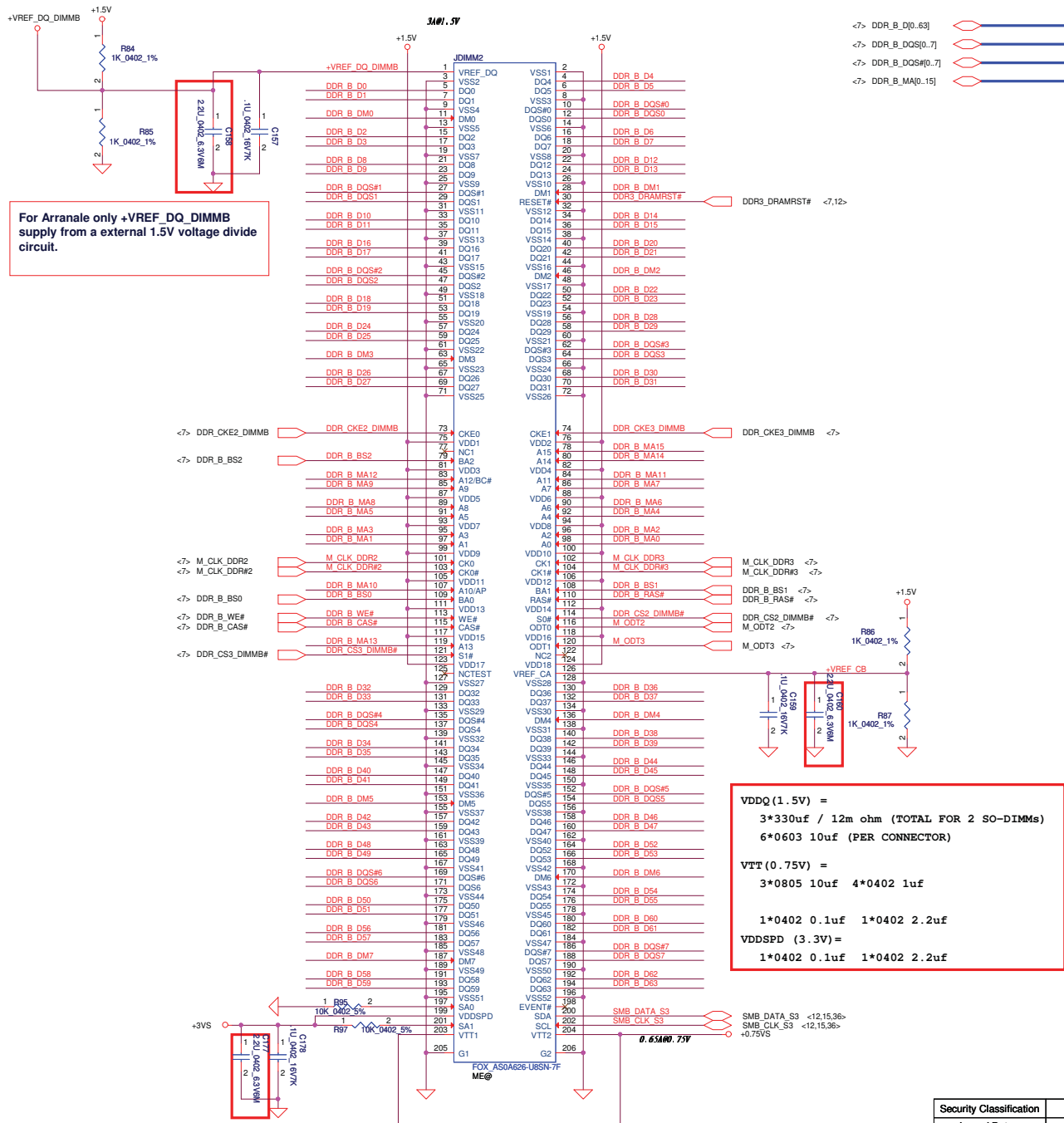
IVY Bridge drives VCCIO\_SEL low  
VCCP\_PWCTRL:0  
Sandy Bridge is NC for A19  
VCCP\_PWCTRL:1

Security Classification	Compal Secret Data			Title
Issued Date	2011/10/27	Deciphered Date	2012/10/27	PROCESSOR(6/7) PWR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-7983P
Date: Thursday, January 05, 2012				Rev 0.3
Sheet 10 of 60				



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	PROCESSOR(7/7) VSS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-7983P
				Date:	Thursday, January 05, 2012
				Sheet	11 of 60
				Rev	0.3





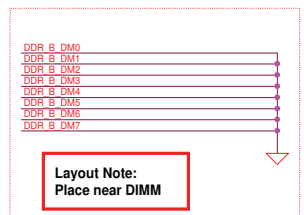
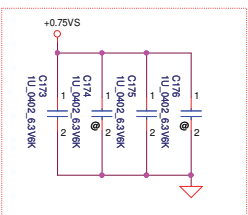
For Arranale only +VREF\_DQ\_DIMMB supply from a external 1.5V voltage divide circuit.

<7> DDR\_B\_D0[0..63]  
<7> DDR\_B\_DQS[0..7]  
<7> DDR\_B\_DQS#0[0..7]  
<7> DDR\_B\_MA[0..15]

Layout Note:  
Place near DIMM

(10uF\_0603\_6.3V) \*8  
(0.1uF\_402\_10V) \*4

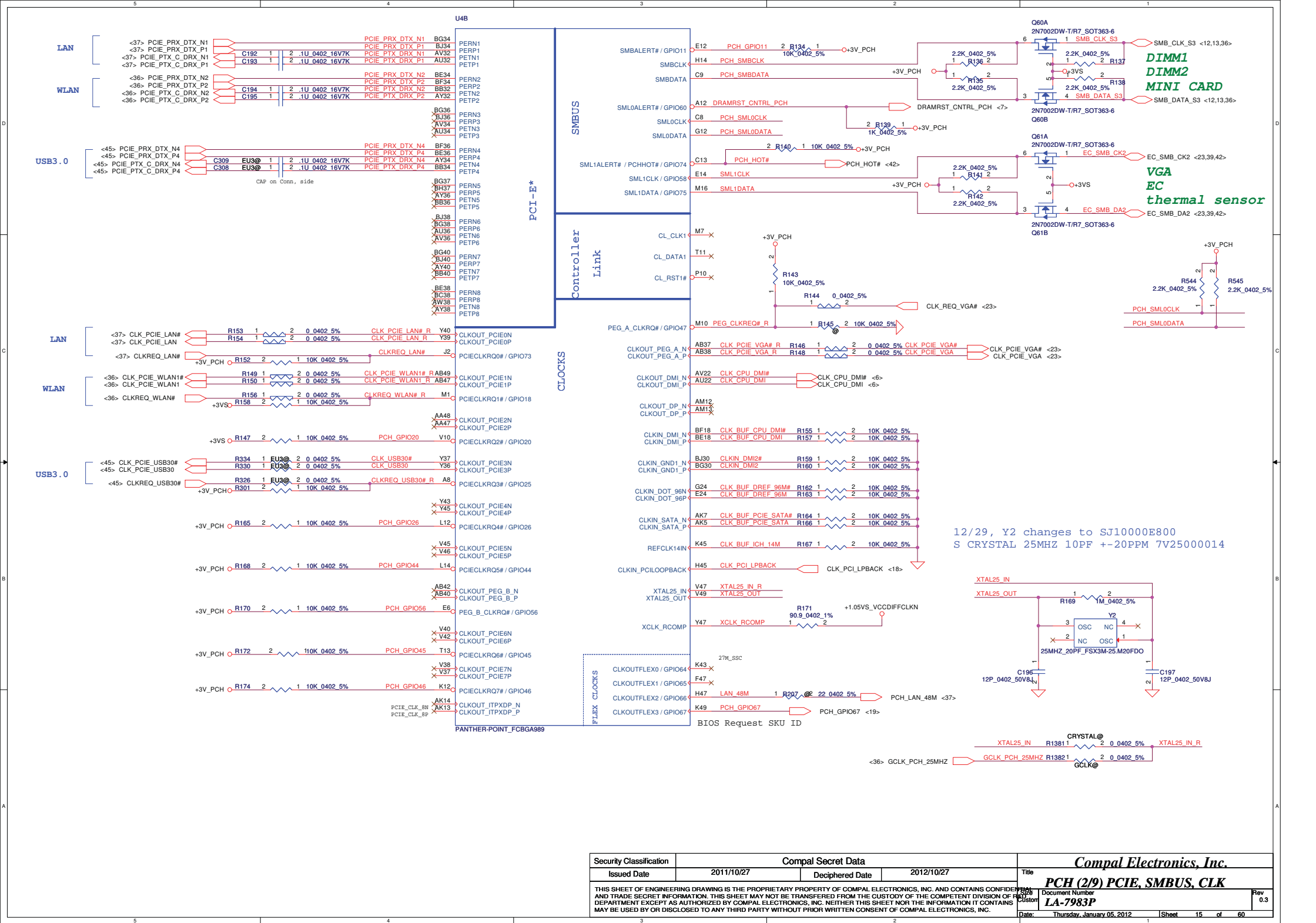
Layout Note:  
Place near DIMM



VDDQ (1.5V) =  
3\*330uF / 12m ohm (TOTAL FOR 2 SO-DIMMs)  
6\*0603 10uF (PER CONNECTOR)  
  
VTT (0.75V) =  
3\*0805 10uF 4\*0402 1uF  
  
VDDSPD (3.3V) =  
1\*0402 0.1uF 1\*0402 2.2uF  
1\*0402 0.1uF 1\*0402 2.2uF

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DDR3-SODIMM SLOT2	
Size		Document Number		Rev	
		LA-7983P		0.3	
Date:		Thursday, January 05, 2012		Sheet 13 of 60	

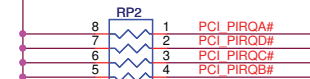




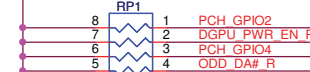




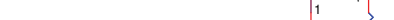
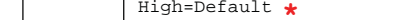
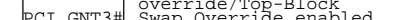
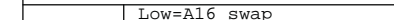
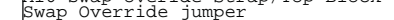
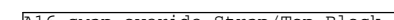
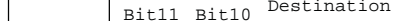
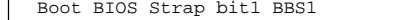
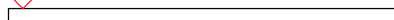
+3VS



8.2K\_0804\_8P4R\_5%



8.2K\_0804\_8P4R\_5%



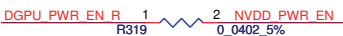
PPT EDS DOC#474146

9/22 NA 9/26 Mount

9/22 from 8.2K NA 9/26 NA

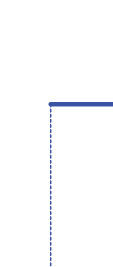
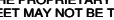
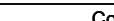
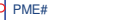
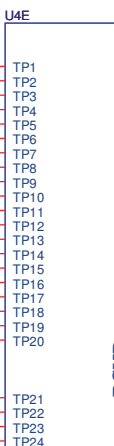
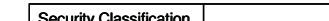
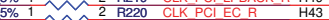
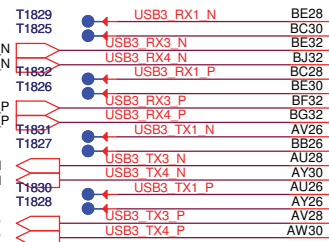
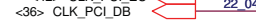
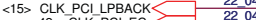
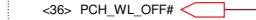
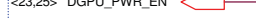
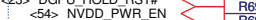
Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	Reserved
	1	1	★ SPI (Default)
	0	0	LPC



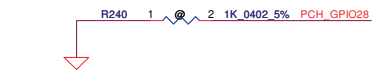
A16 swap override Strap/Top-Block Swap Override jumper

PCI\_GNT3# Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

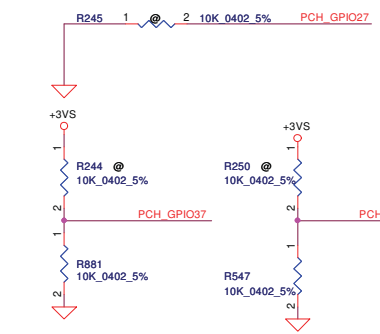




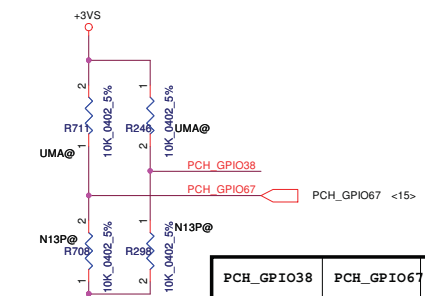
GPIO28  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
★ H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable



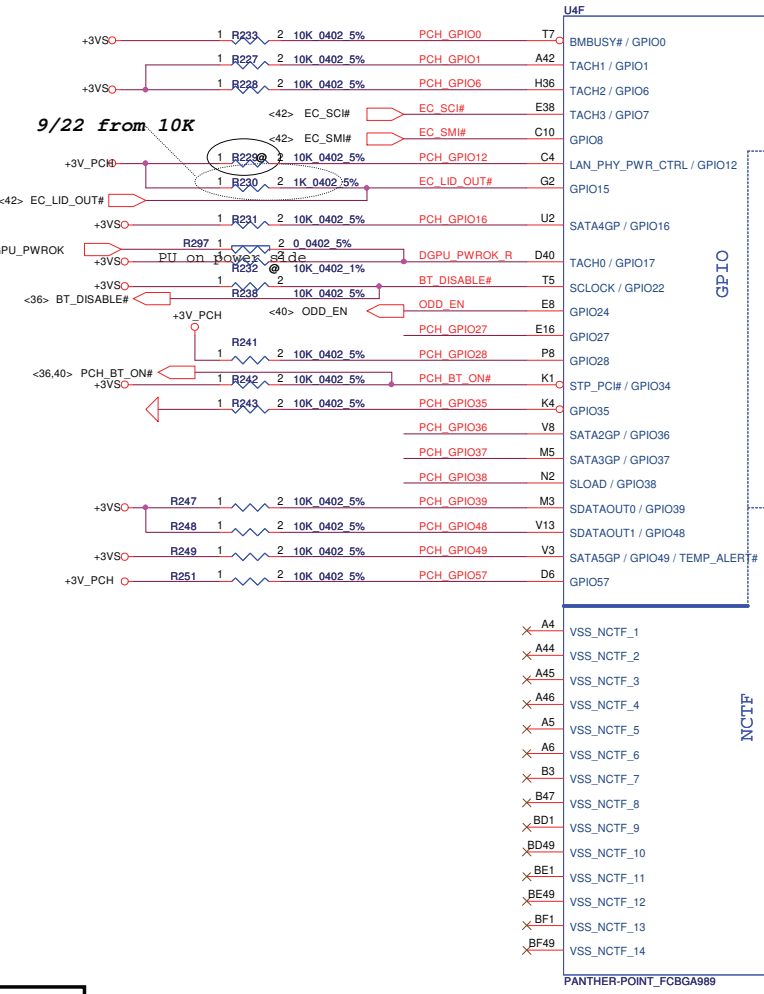
★ PCH\_GPIO27 (Have internal Pull-High)  
High: VCCVRM VR Enable  
Low: VCCVRM VR Disable



BIOS Request SKU ID

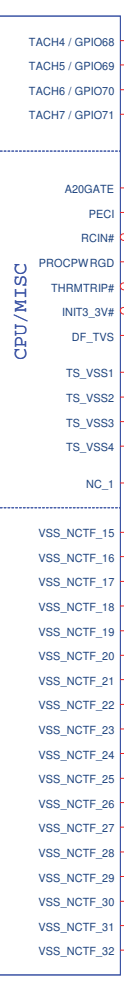


PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

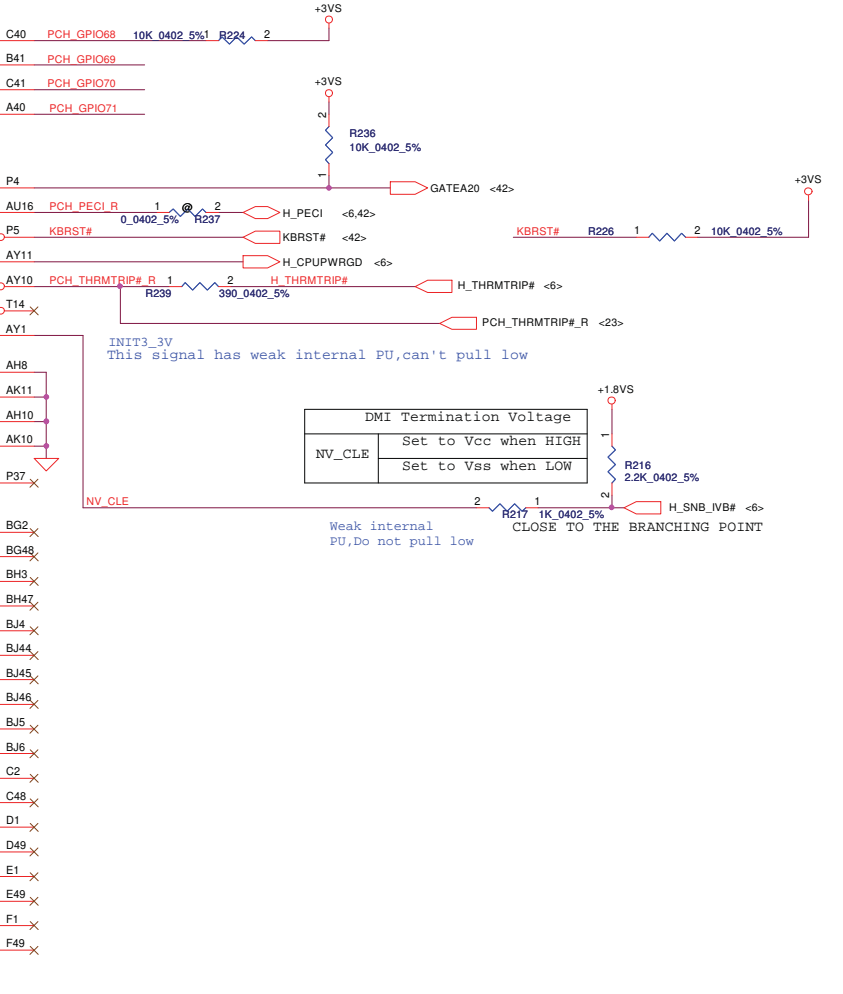


GPIO

NCTF



CPU/MISC

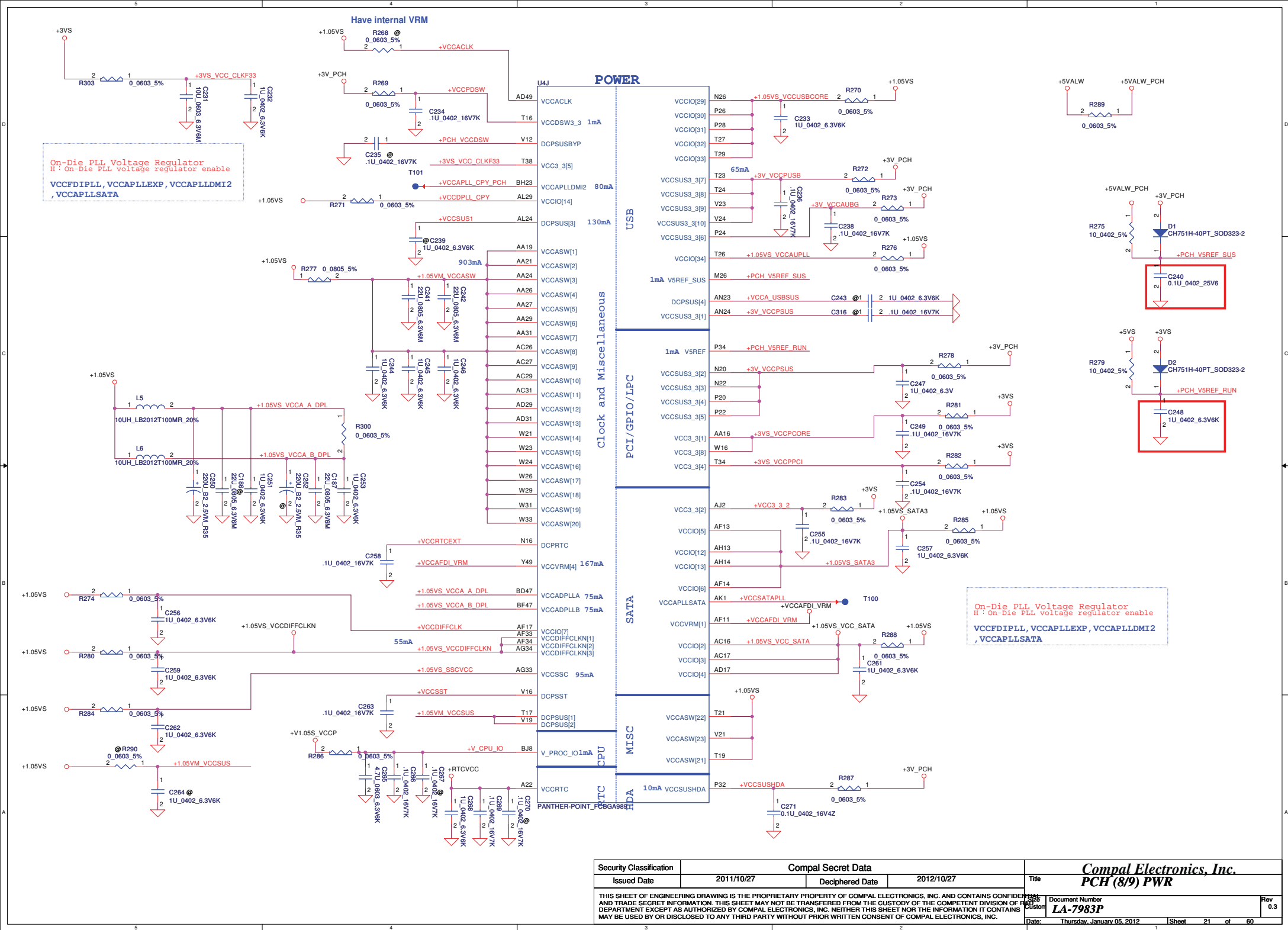


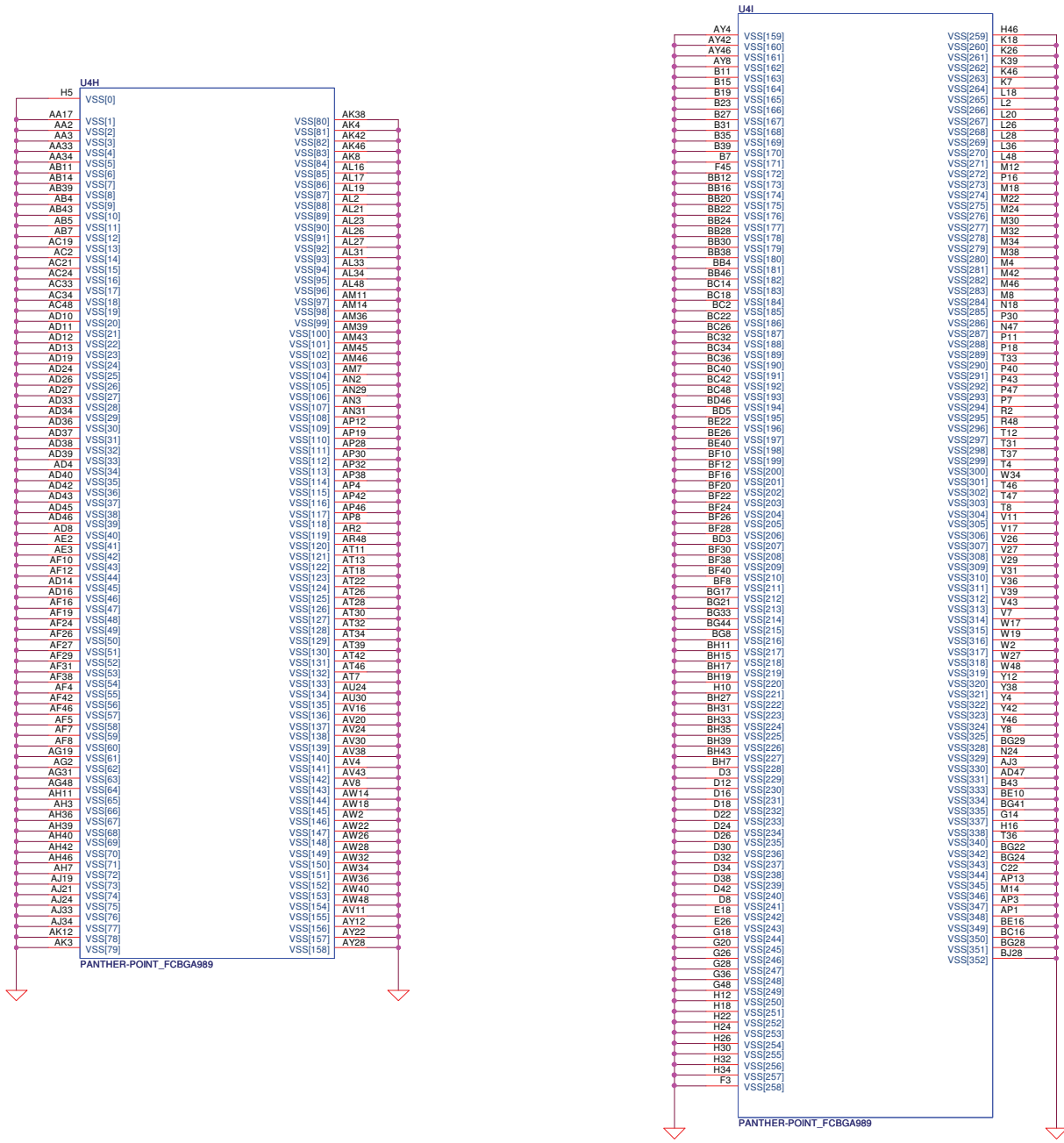
PCH_GPIO70	Function
0	14/15"
1	17"
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

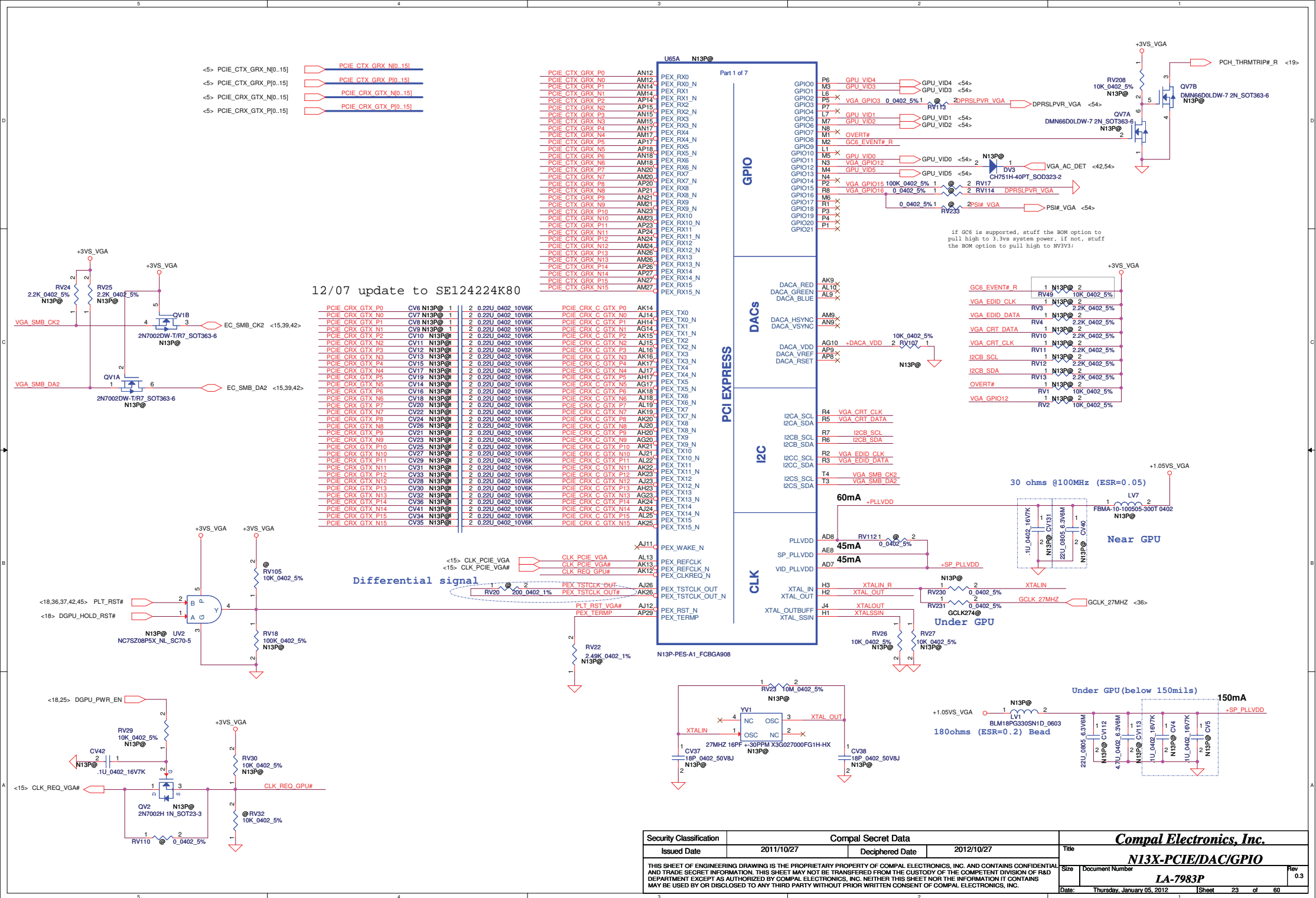
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

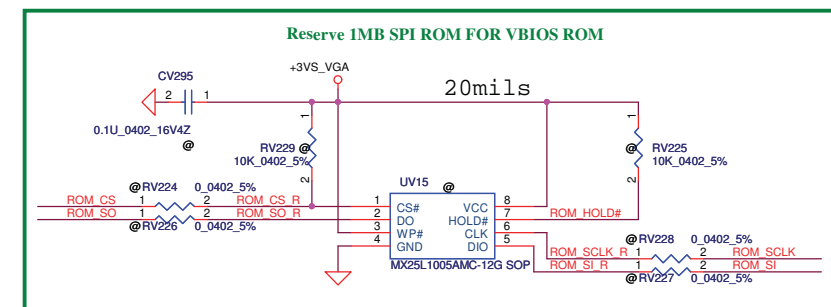
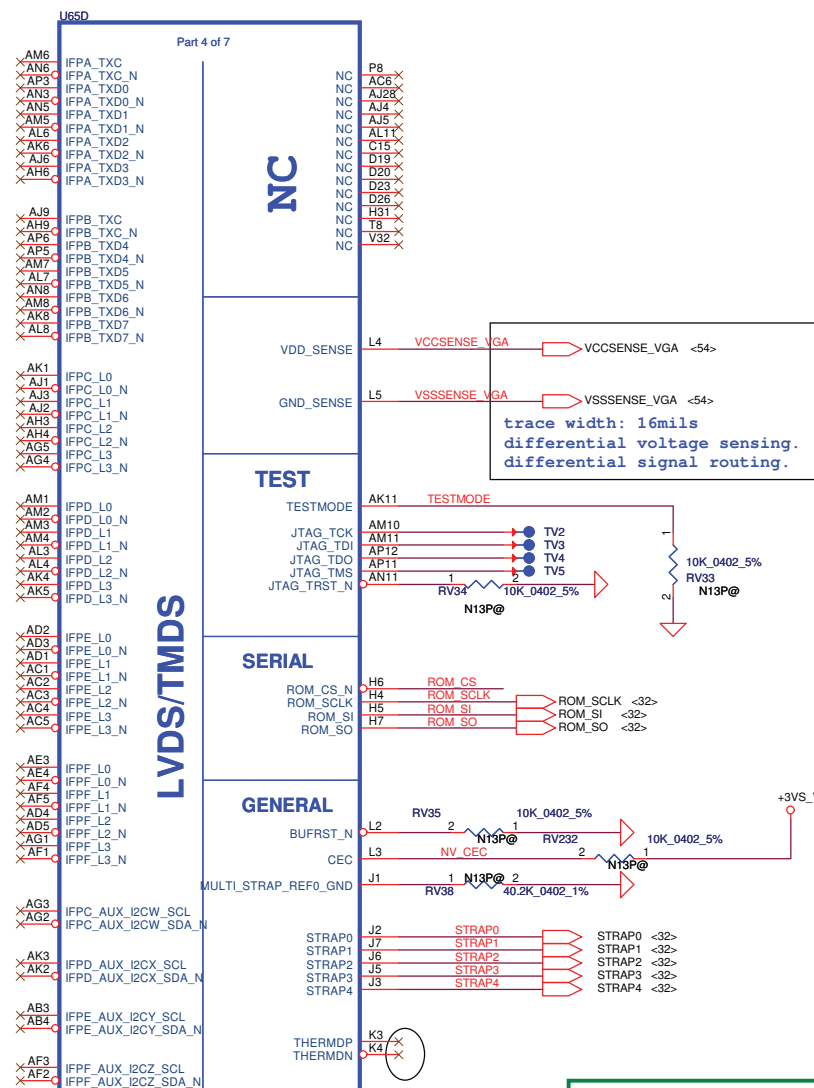
Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Size	Custom
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date	Thursday, January 05, 2012
				Sheet	19 of 60





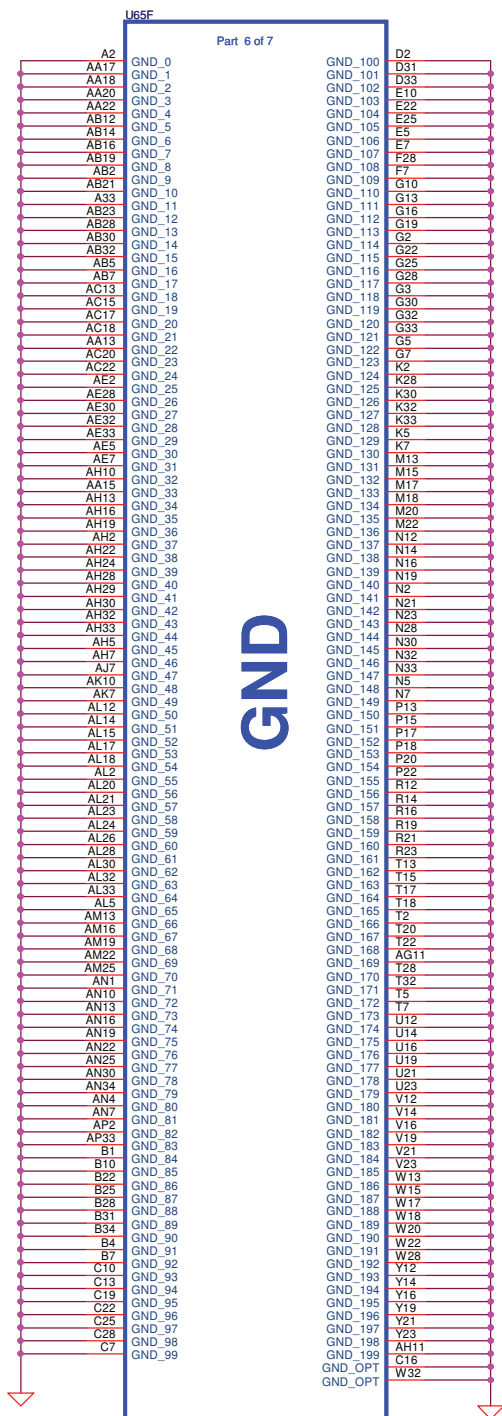






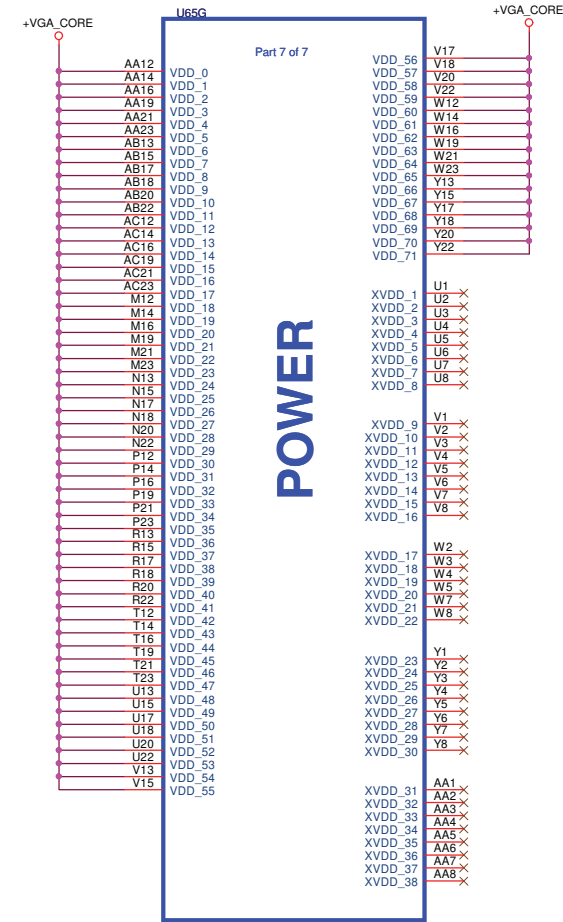
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	N13X-LVDS/HDMI/DP/THM	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-7983P	0.3
				Date	Thursday, January 05, 2012	Sheet 24 of 60





N13P-PES-A1\_FCBGA908

N13P@

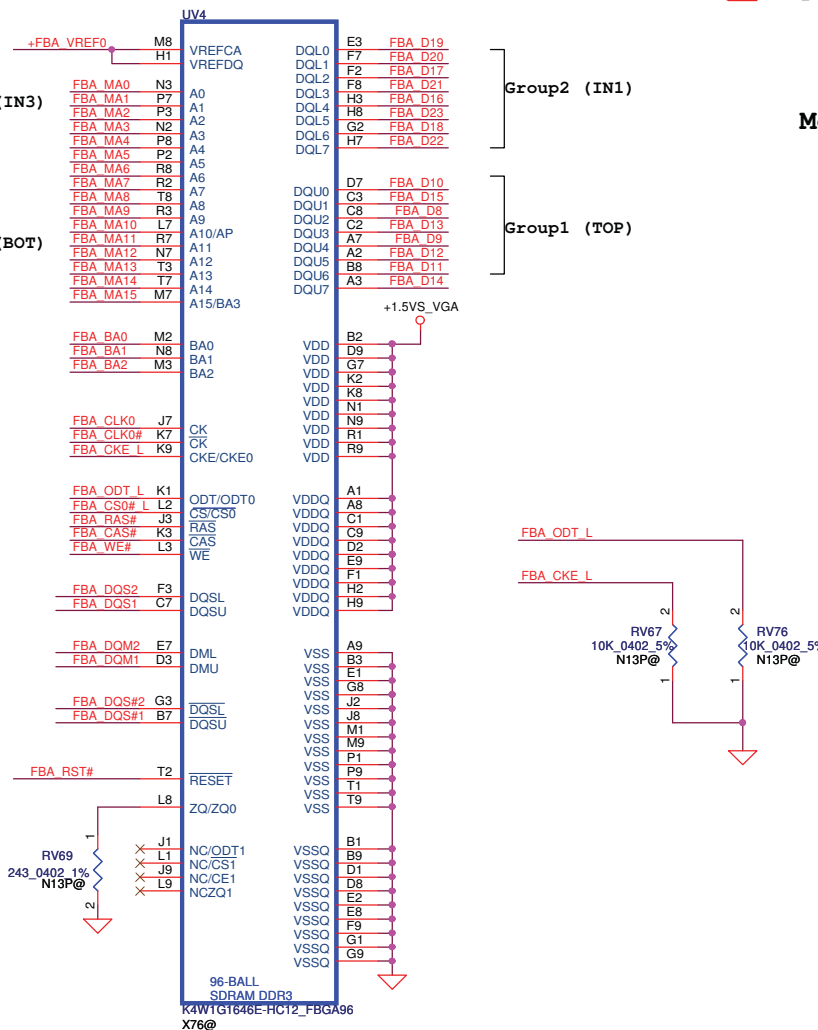


N13P-PES-A1\_FCBGA908

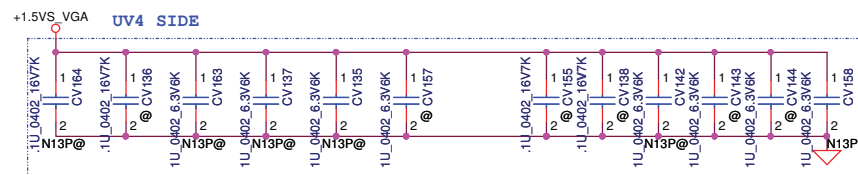
N13P@

Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>							
Issued Date		2011/10/27		Deciphered Date		2012/10/27		Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								<b>N13-VGA CORE, GND</b>					
								Size		Document Number		Rev	
										<b>LA-7983P</b>		0.3	
								Date:		Thursday, January 05, 2012		Sheet 26 of 60	



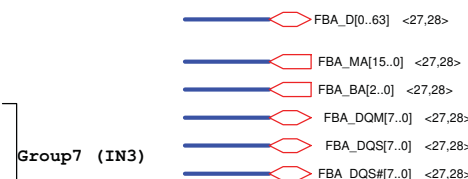
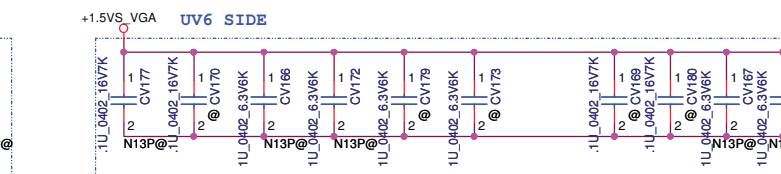
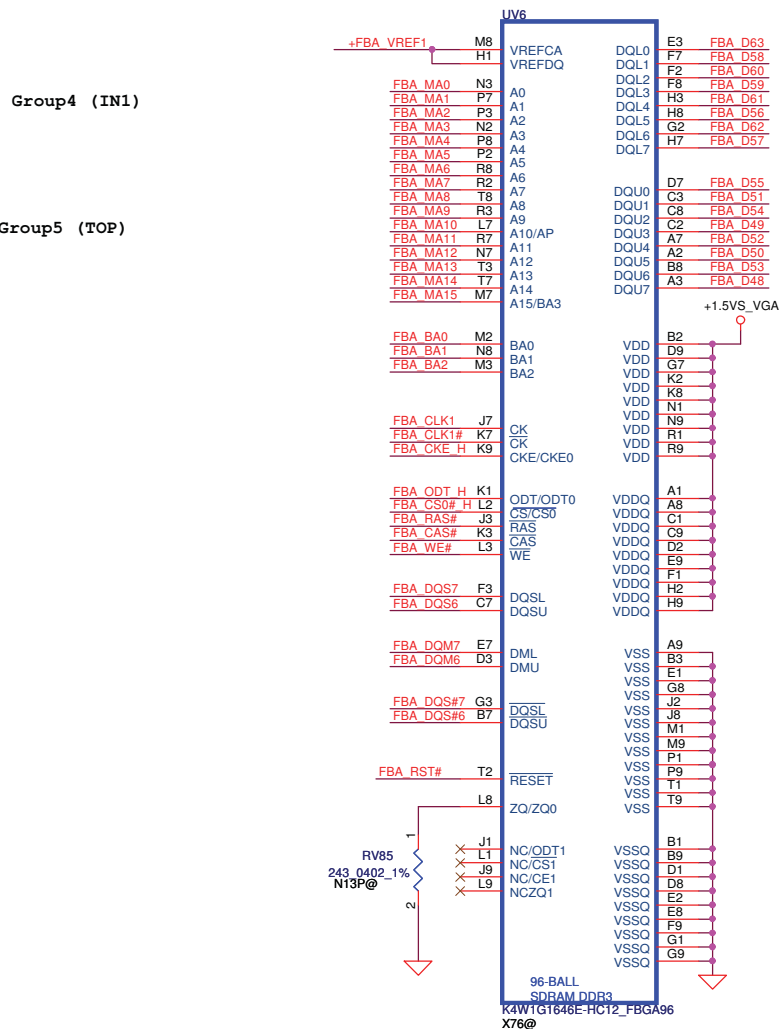
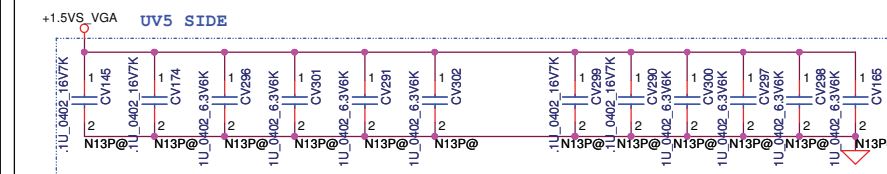
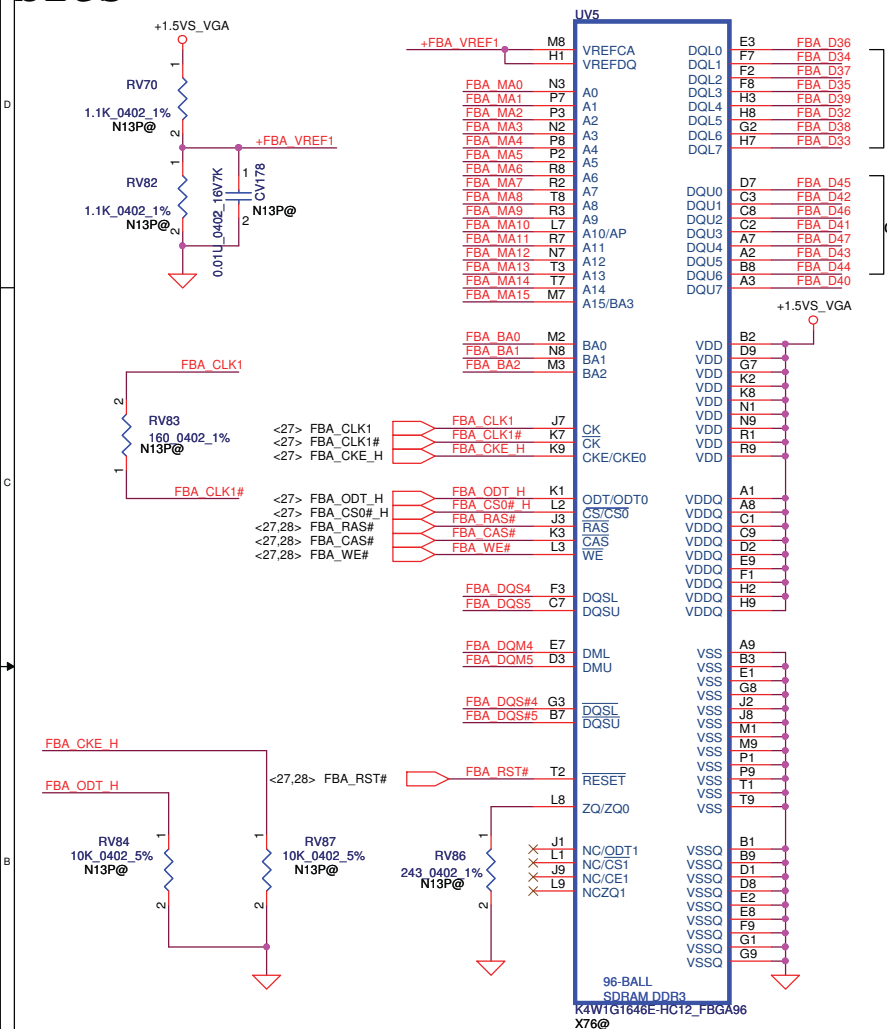


	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



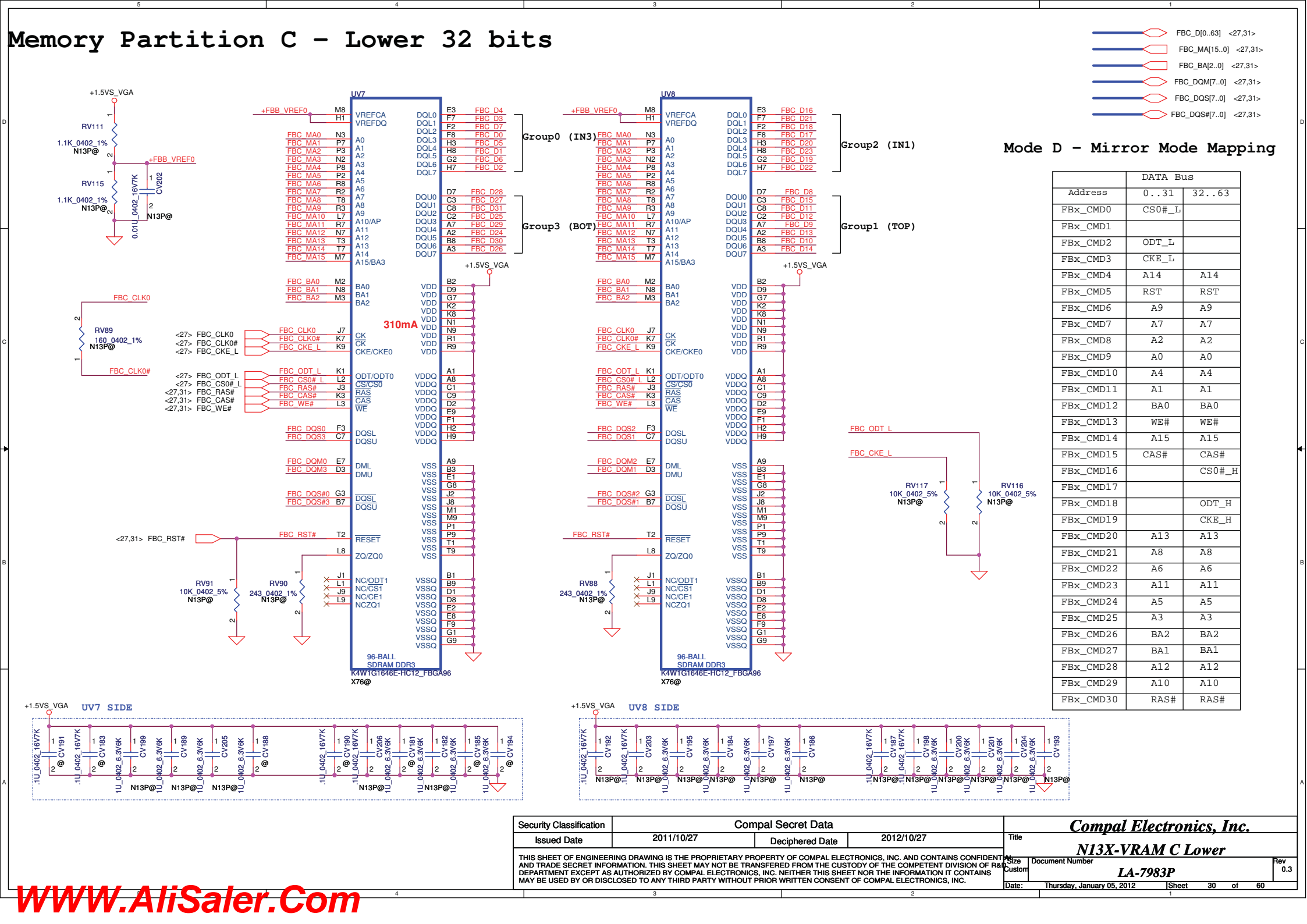
**WWW.AliSaler.Com**

Memory Partition A - Upper 32 bits



## Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

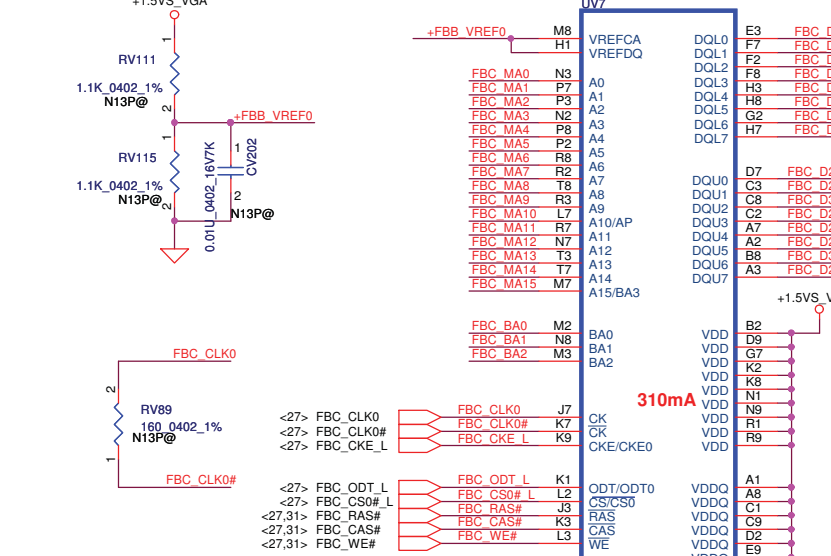
[illegible]

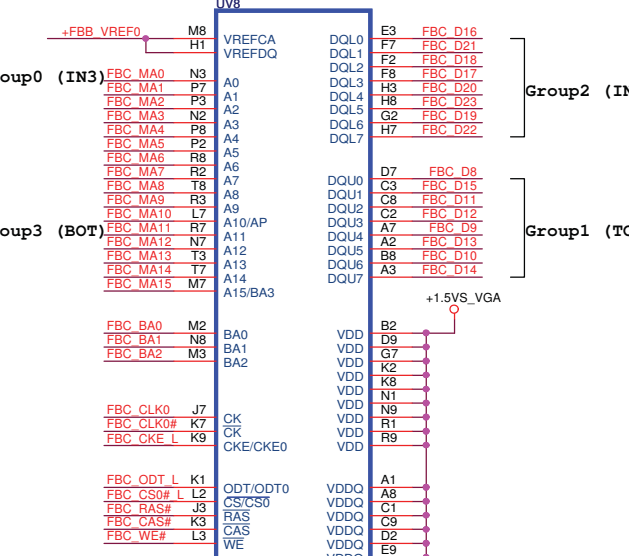
# Memory Partition C - Lower 32 bits

FBC\_D[0..63] <27,31>  
FBC\_MA[15..0] <27,31>  
FBC\_BA[2..0] <27,31>  
FBC\_DQM[7..0] <27,31>  
FBC\_DSQ# [7..0] <27,31>

## Mode D - Mirror Mode Mapping

Address	Data Bus
FBx_CMD0	CS0#_L
FBx_CMD1	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	ODT_H
FBx_CMD19	CHE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

UV7 SIDE  


UV8 SIDE  


+1.5VS\_VGA

UV7

K4W1G1646E-HC12\_FBGAg6 X76@

+1.5VS\_VGA

UV8

K4W1G1646E-HC12\_FBGAg6 X76@

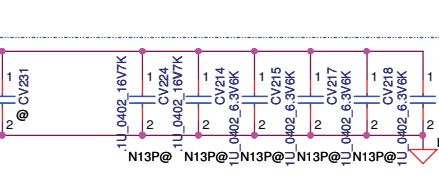
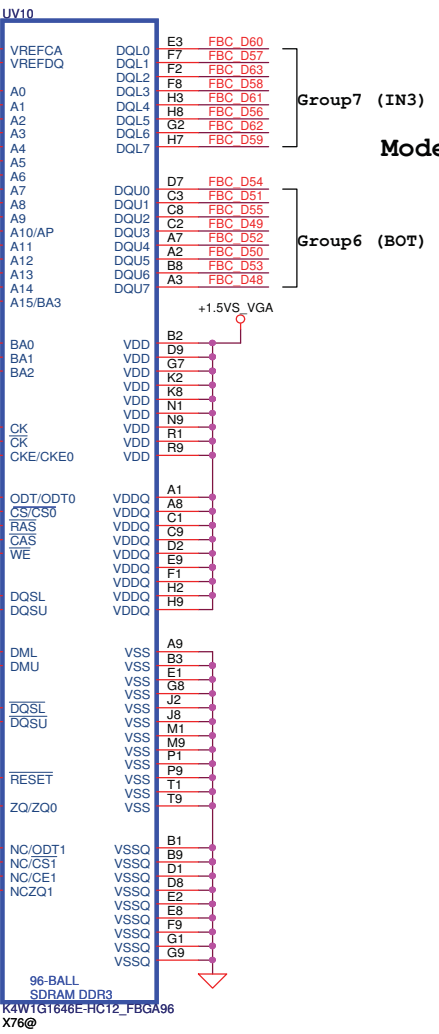
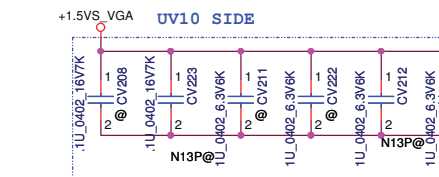
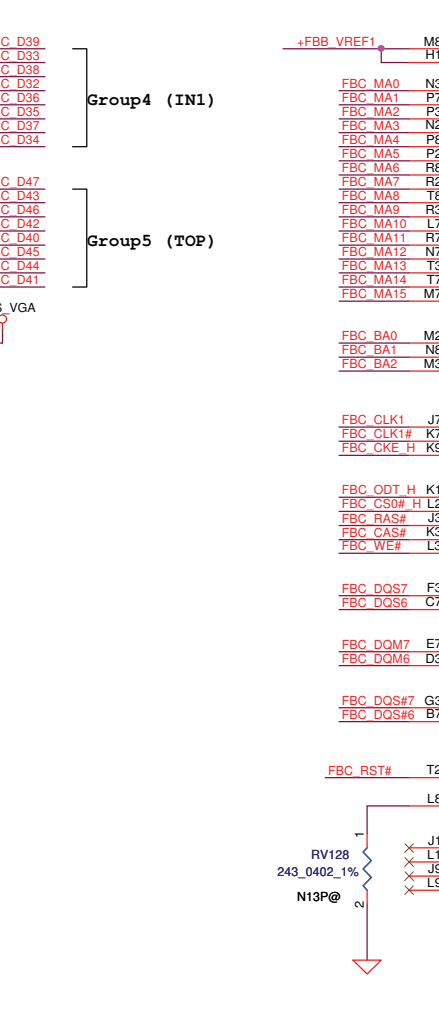
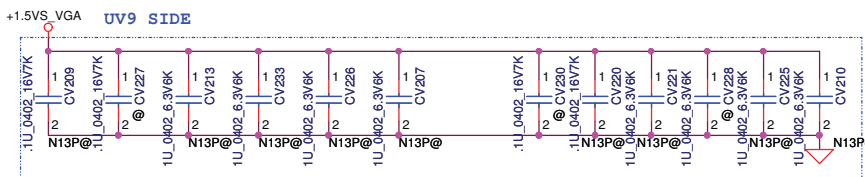
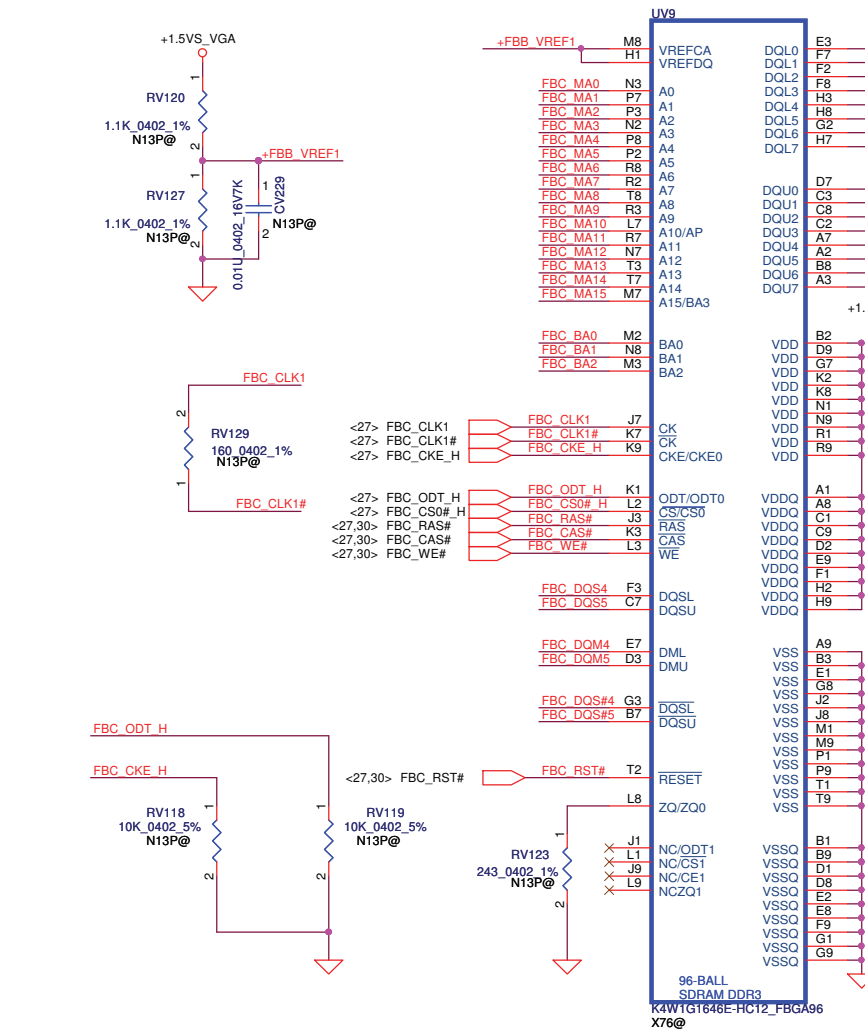
This sheet contains information that may be controlled under U.S. export control laws.

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

WWW.AliSaler.Com

[illegible]

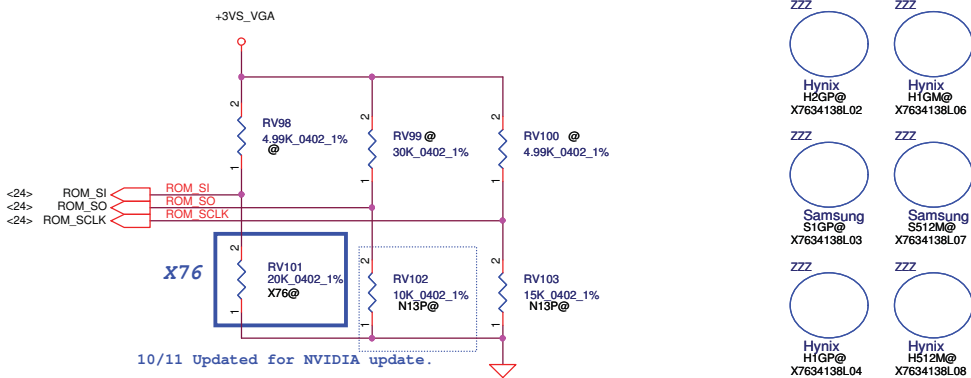
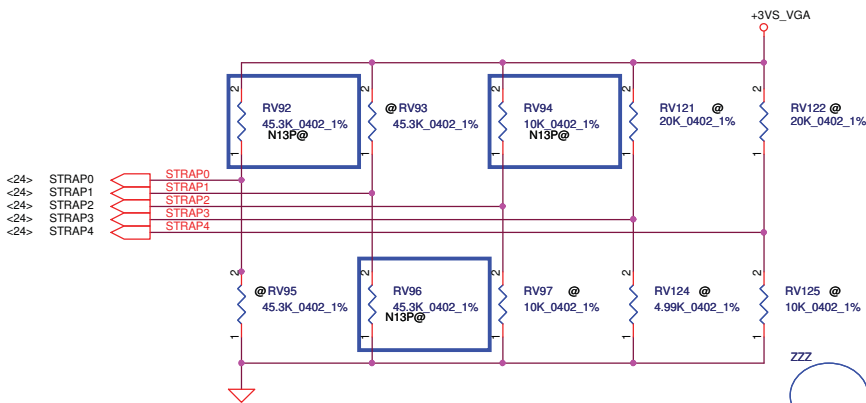
Memory Partition C - Upper 32 bits



- FBC\_D[0..63] <27,30>
- FBC\_MA[15..0] <27,30>
- FBC\_BA[2..0] <27,30>
- FBC\_DQM[7..0] <27,30>
- FBC\_DQS[7..0] <27,30>
- FBC\_DQS# [7..0] <27,30>

Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	
FBx_CMD17	CS0#_H
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#



For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16" 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16" 8 2GB	Hynix (2Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16" 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16" 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 45K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

10/11 Updated for NVIDIA update.

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

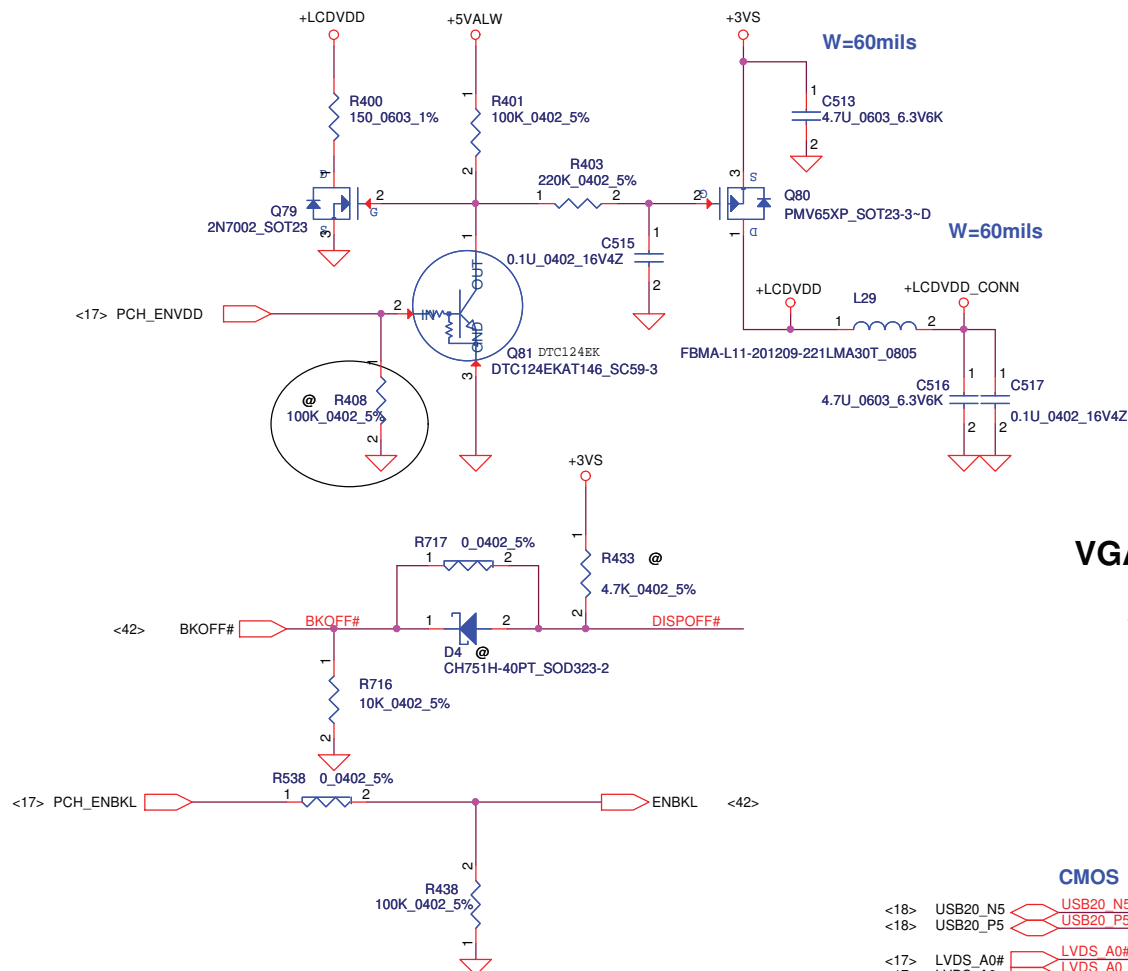
PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/10/27		Deciphered Date		2012/10/27		Title	
										N13X MISC	
										LA-7983P	
										Rev 0.3	
										Date: Thursday, January 05, 2012	
										Sheet 32 of 60	

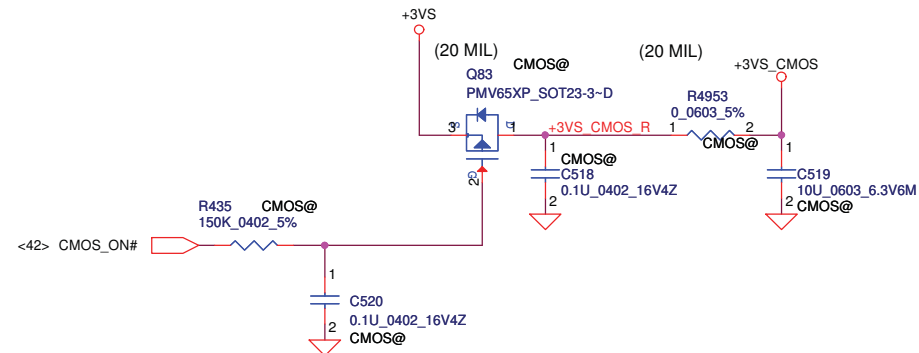
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size Custom  
Document Number  
Date: Thursday, January 05, 2012  
Sheet 32 of 60

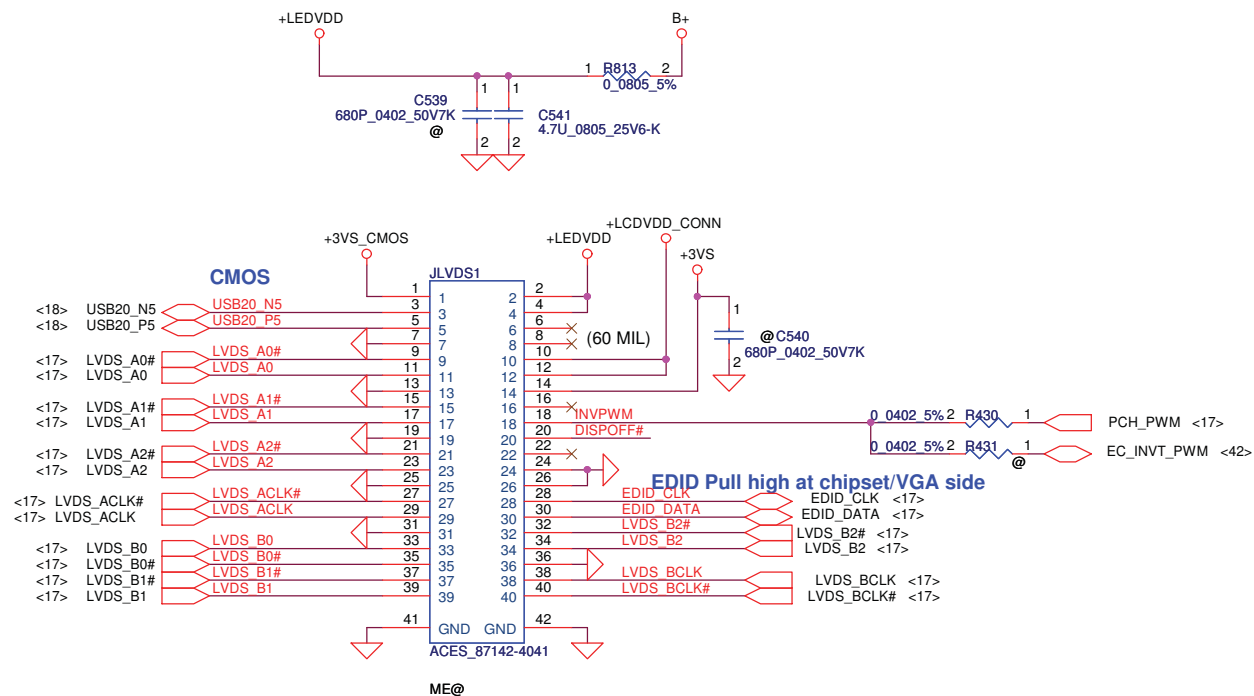
# LCD POWER CIRCUIT



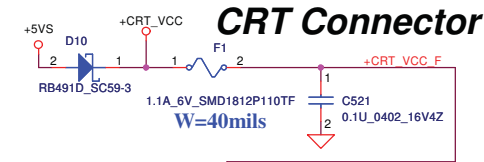
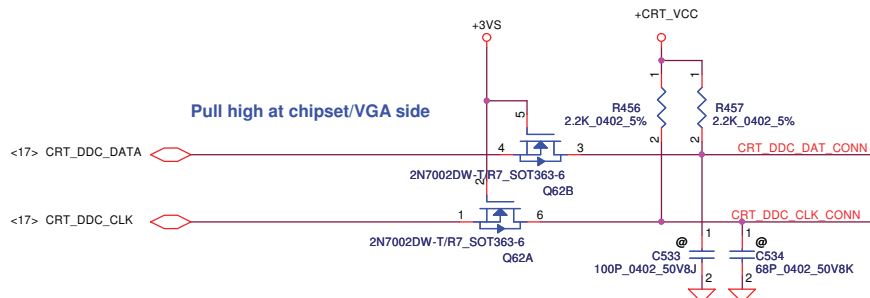
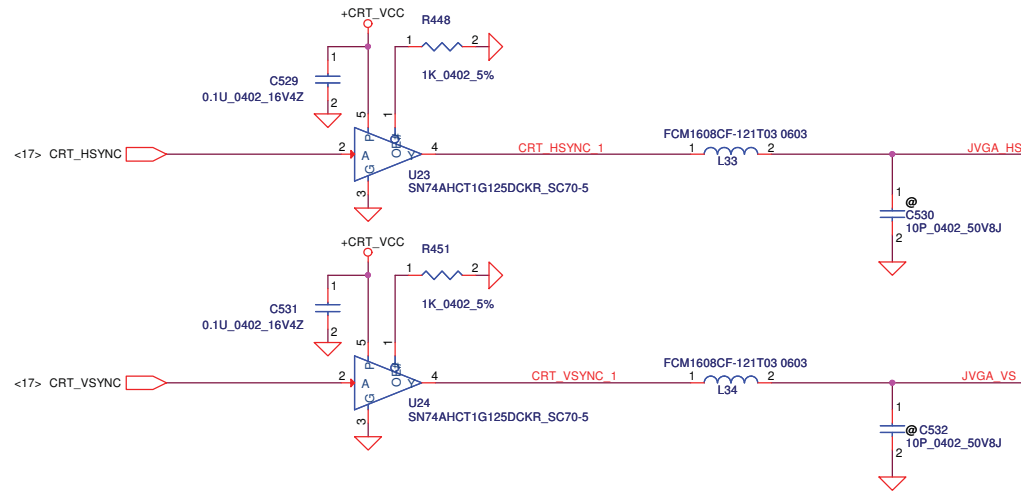
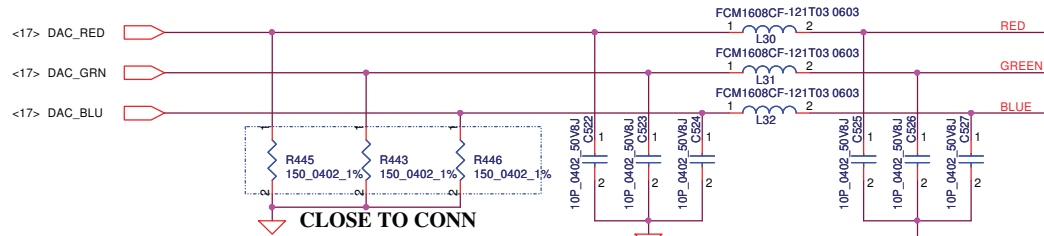
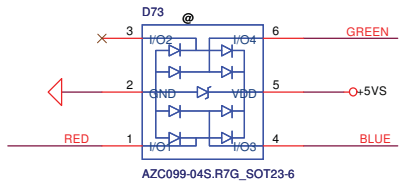
# CMOS Camera



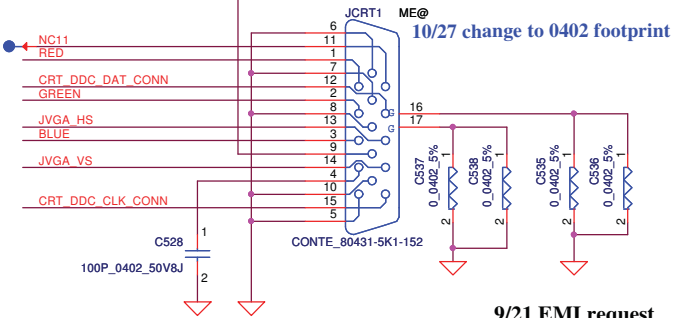
# VGA LCD/PANEL BD. Conn.



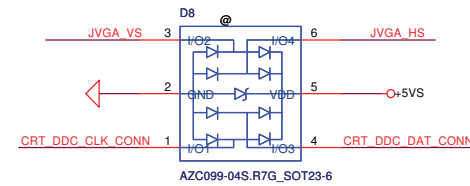
Security Classification	Compal Secret Data		Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Custom
				LA-7983P
				Rev 0.3
				Date: Thursday, January 05, 2012
				Sheet 33 of 60



PAD T66



9/21 EMI request  
0ohm and mount

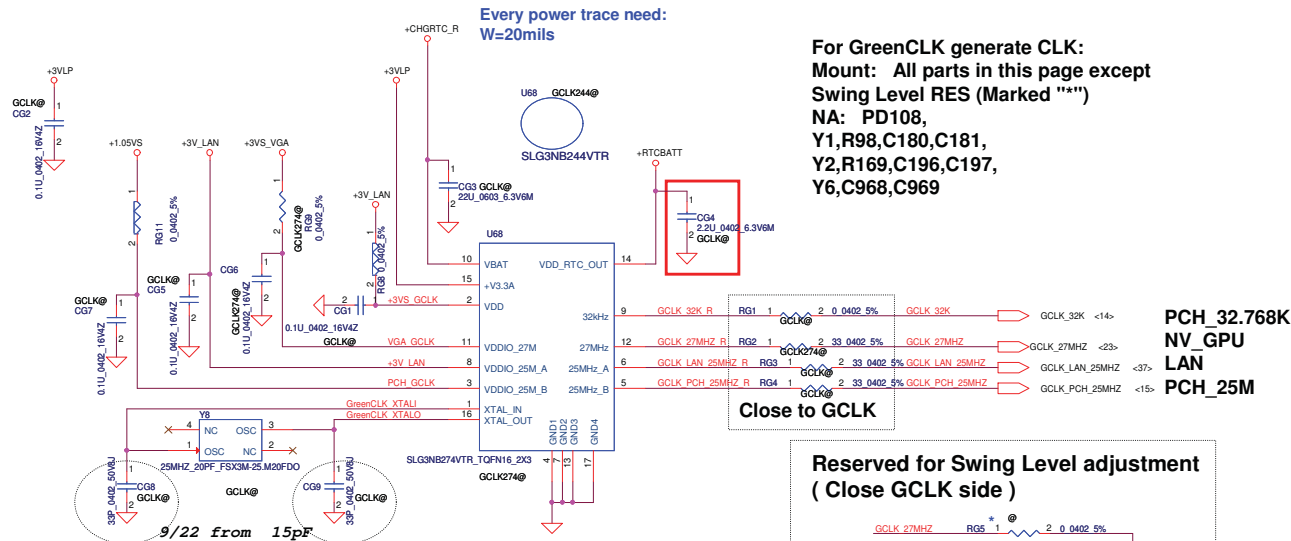
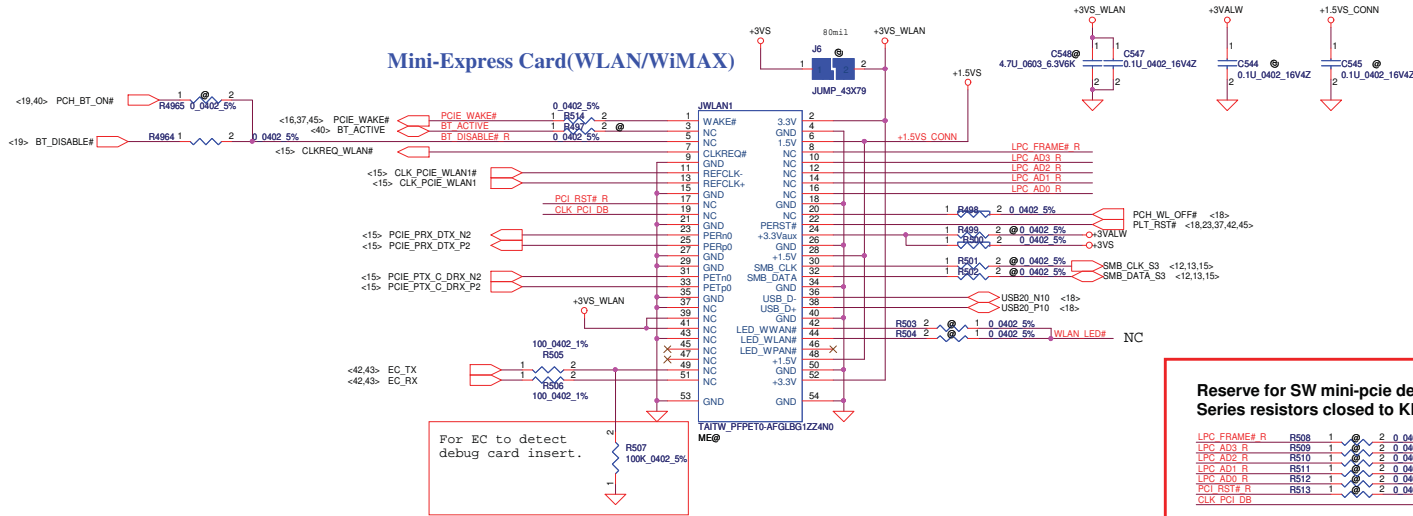


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	<b>CRT Connector</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number <b>LA-7983P</b>
				Date: Thursday, January 05, 2012	Rev 0.3
				Sheet 34 of 60	



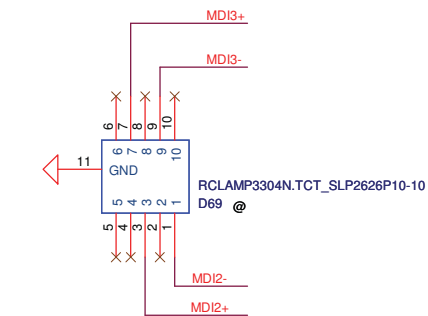
# Mini-Express Card for WLAN/WiMAX(Half)

## Mini-Express Card(WLAN/WiMAX)

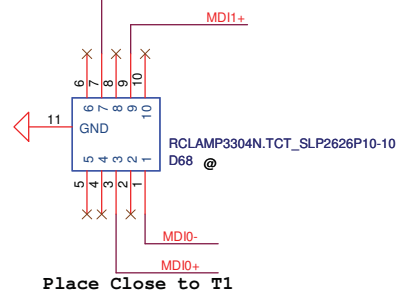


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Mini-Card/Green CLK
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Document Number
				LA-7983P
				Rev 0.3
				Date: Thursday, January 05, 2012 Sheet 36 of 60



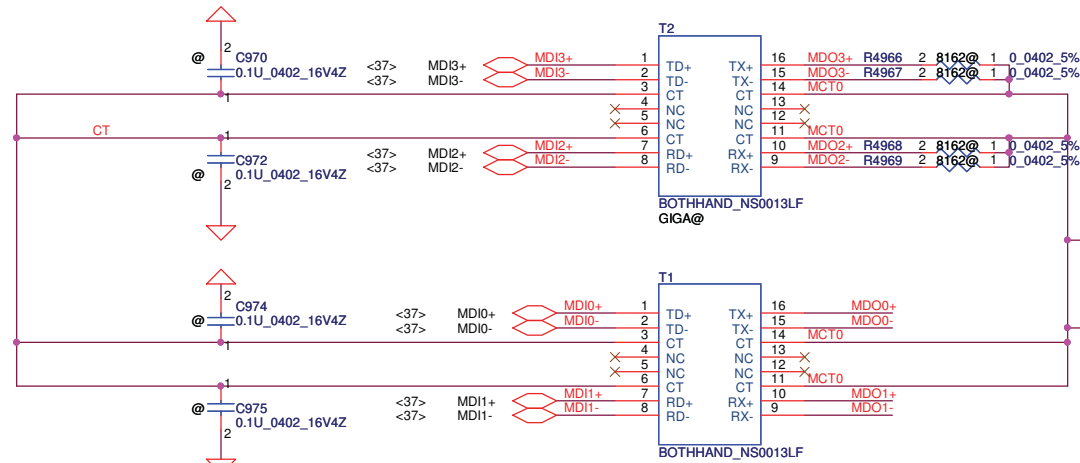


Place Close to T2

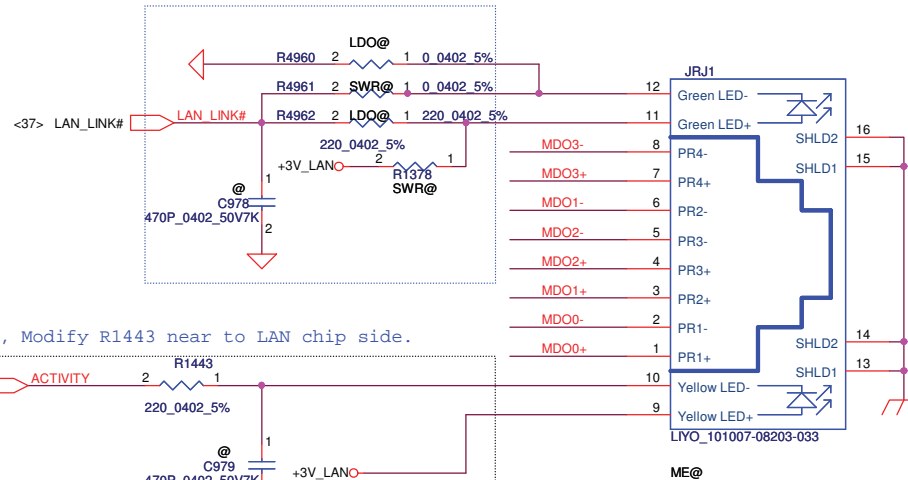


Place Close to T1

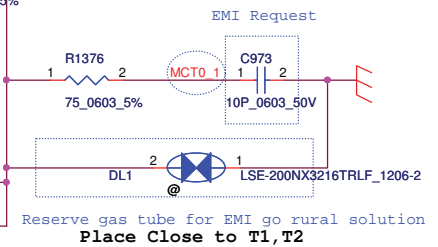
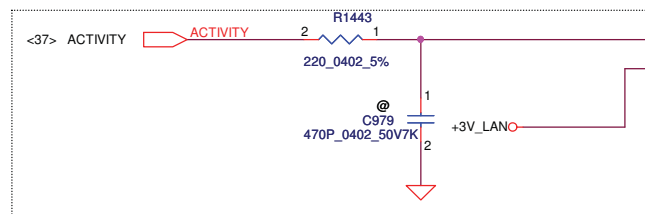
T1,T2 P/N to SP050007K00



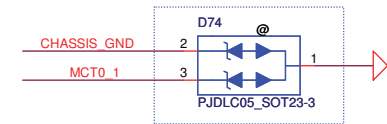
SWR or LDO Mode Update



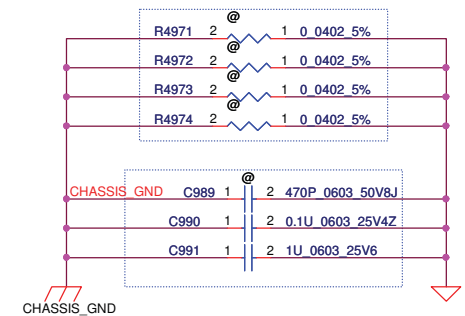
For ESD surge, Modify R1443 near to LAN chip side.



For ESD request, 10/26 update reserved

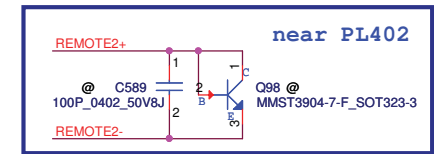
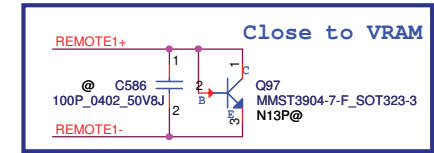
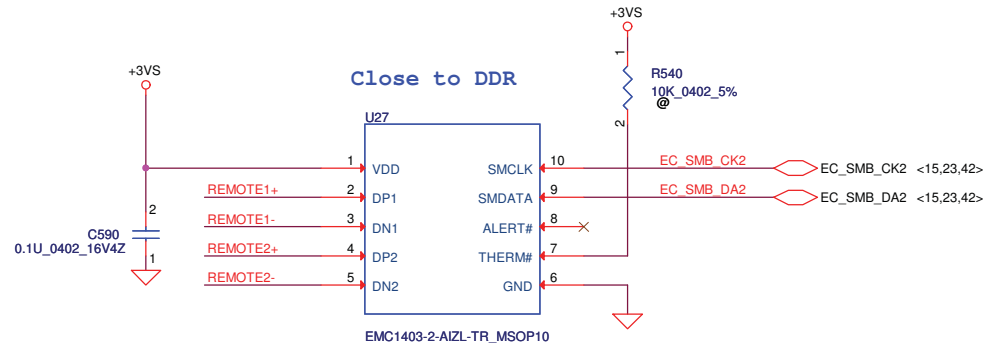
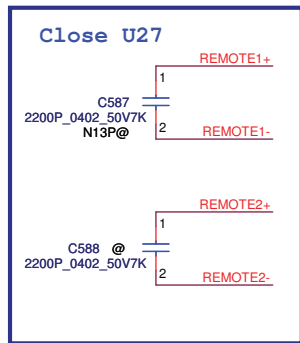


For EMI request, 10/27 update reserved

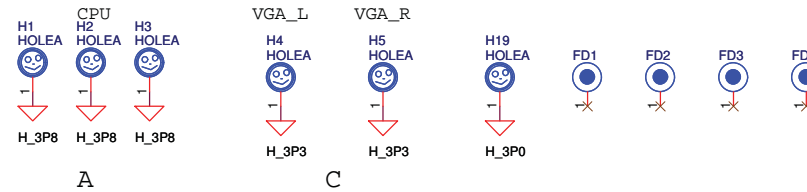


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/10/27				Deciphered Date			
2011/10/27				2012/10/27				Title			
2012/10/27				LAN_Transformer				Document Number			
LA-7983P				Rev				0.3			
Date:				Thursday, January 05, 2012				Sheet			
38				of				60			

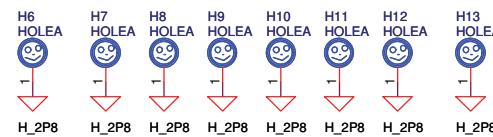
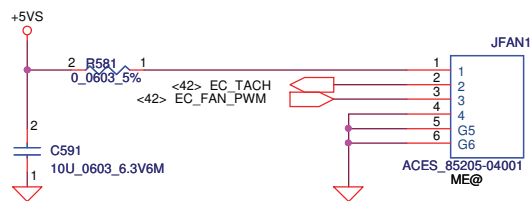
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



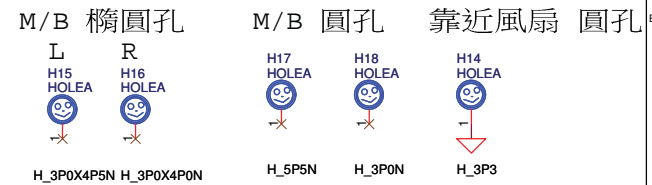
**REMOTE1,2+/-:**  
Trace width/space:10/10 mil  
Trace length:<8"



## FAN1 Conn

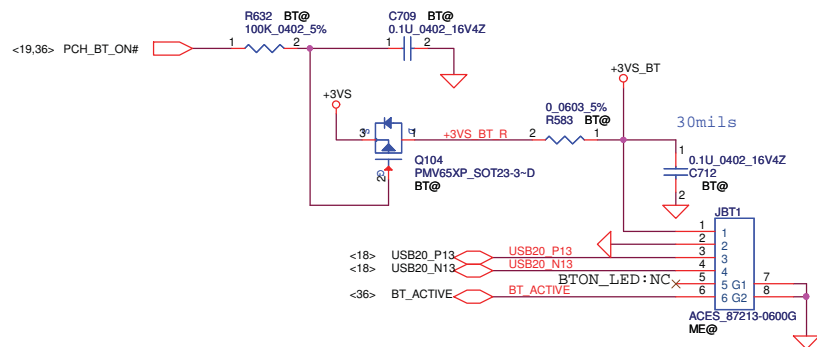


**B**  
2P8 \* 8pcs

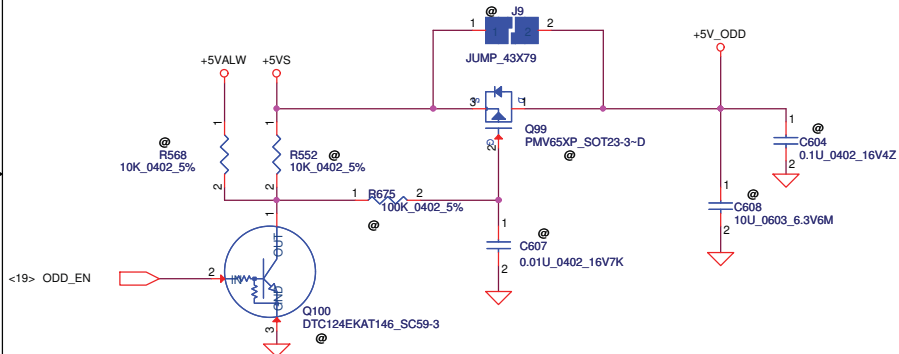


Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	Fintek-Thermal IC/FAN/screw
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7983P
				Date: Thursday, January 05, 2012	Sheet 39 of 60

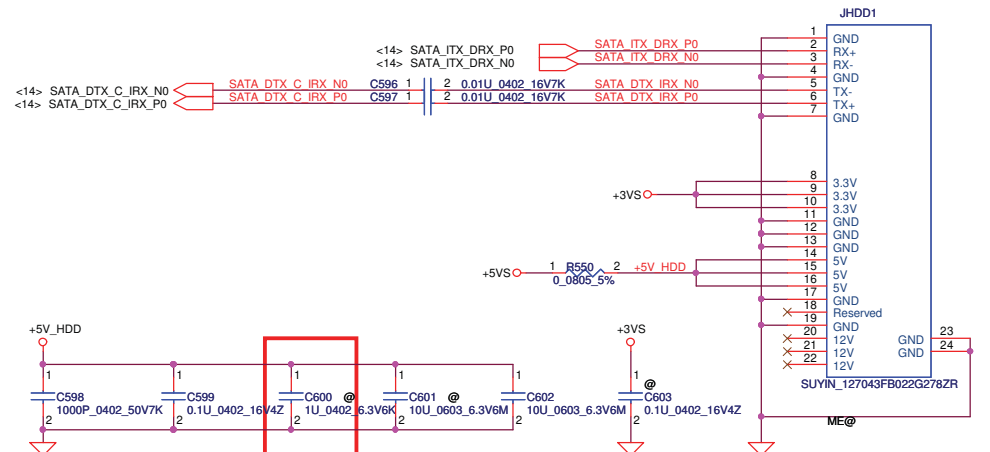
## BT MODULE CONN



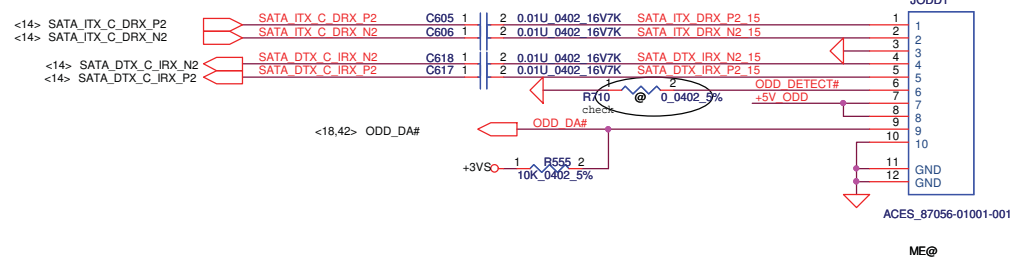
## ODD Power Control



**SATA HDD Conn.**

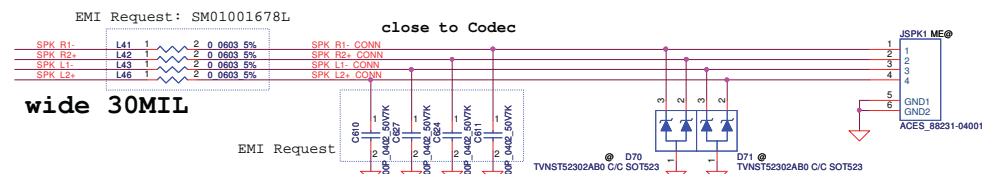
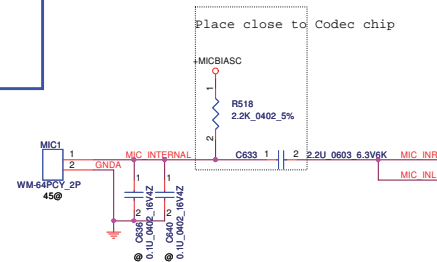
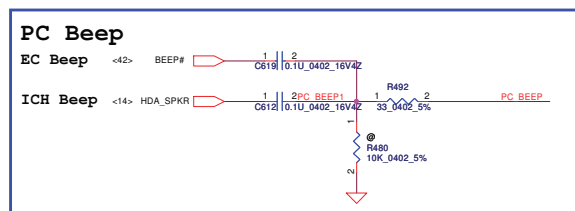
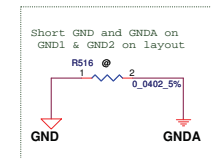
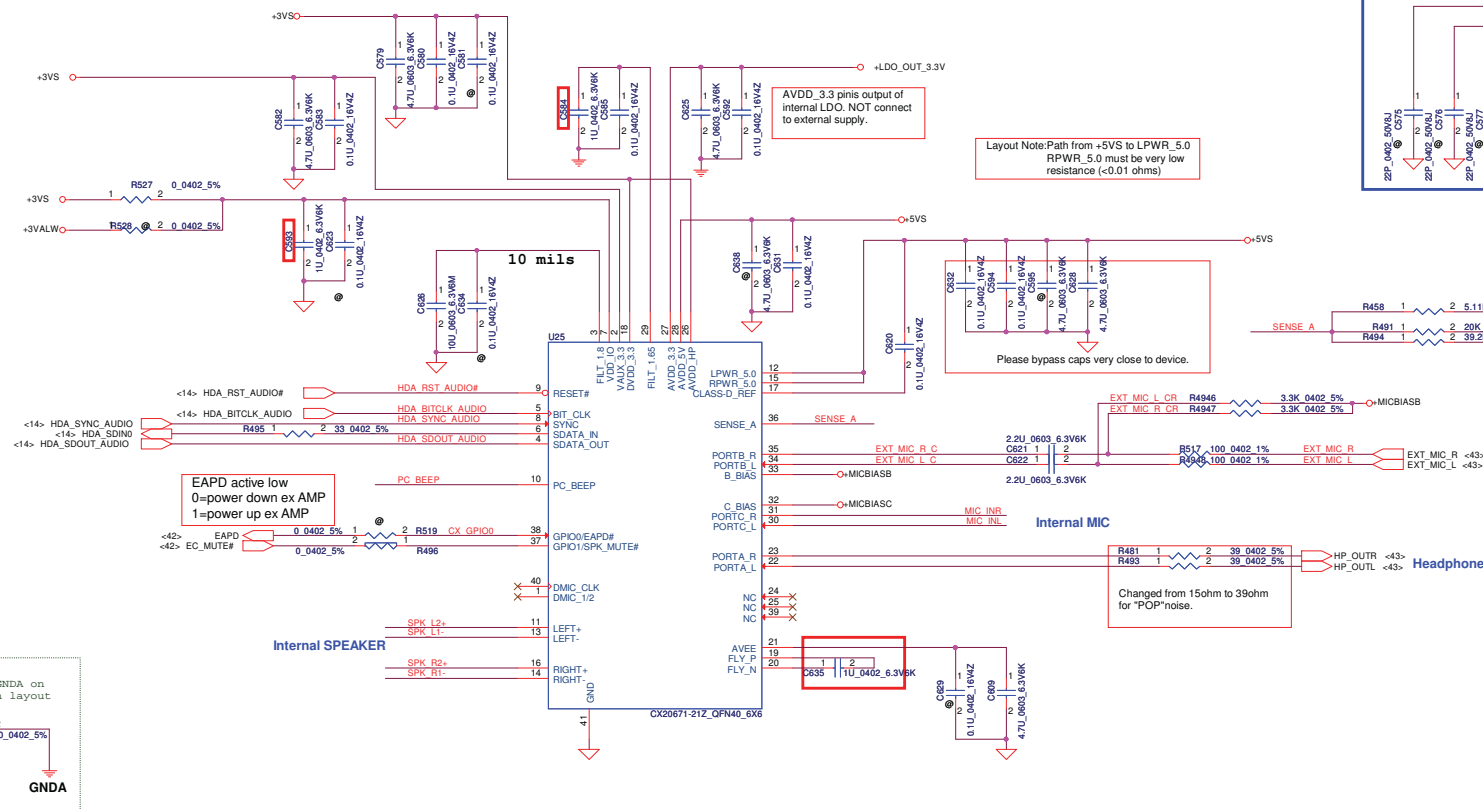


**SATA ODD FFC Conn.**



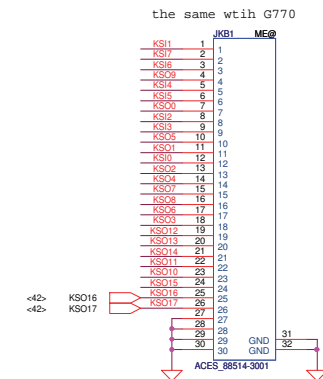
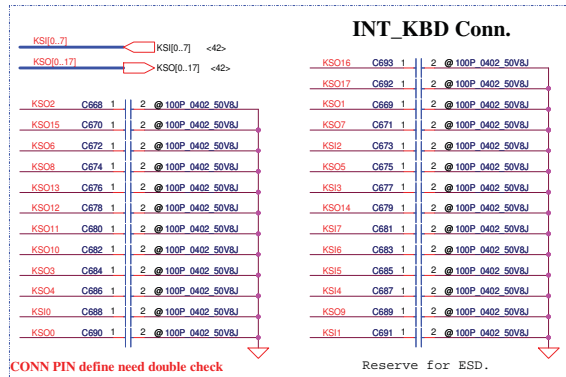
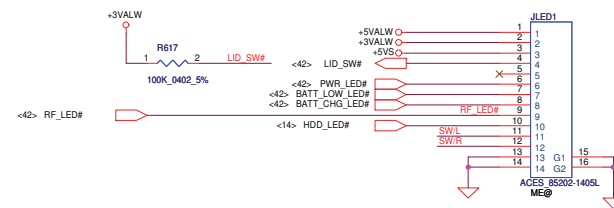
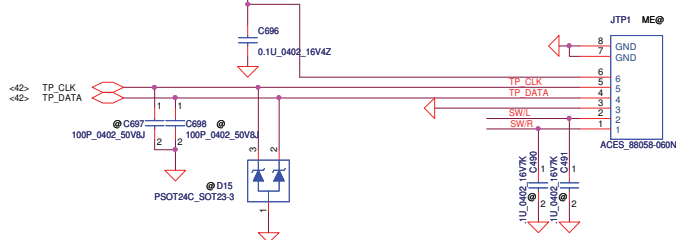
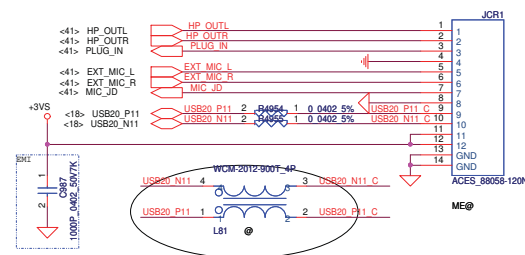
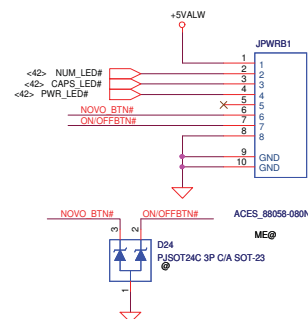
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HDD/ODD/BT Connector</b>	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Custom Document Number <b>LA-7983P</b>	Rev 0.3
				Date: Thursday, January 05, 2012	Sheet 40 of 60

CX20671  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.  
An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).



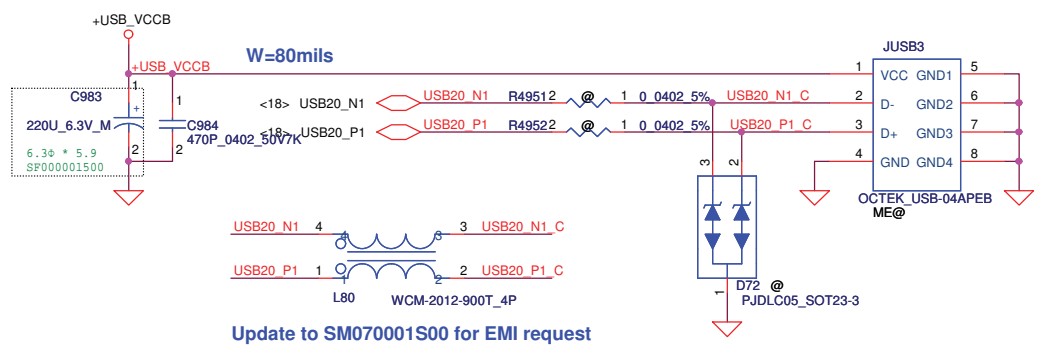
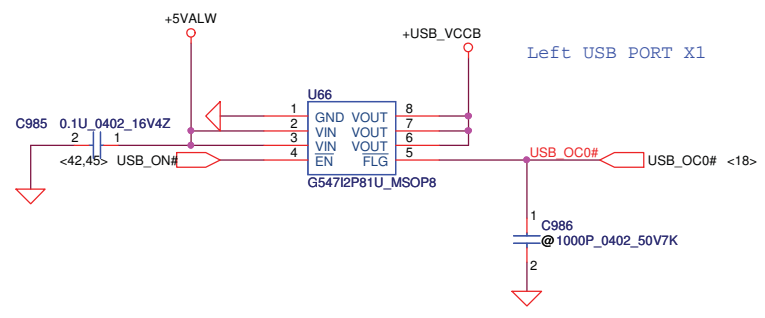
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	CX20671 Codec
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-7983P
Date: Thursday, January 05, 2012				Sheet	41 of 60



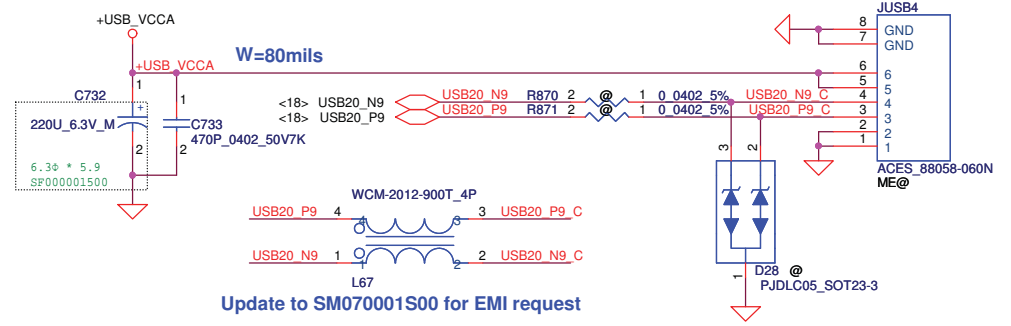
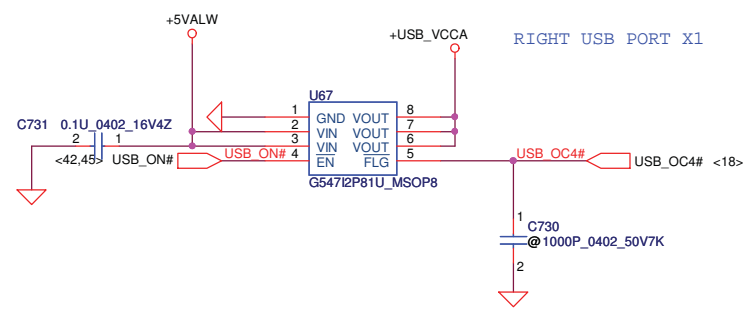
**Card Reader/Audio Jack SB CONN**

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>ROM/KBD/PWR/CR/LED/TP Conn.</b>	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C	Document Number <b>LA-7983P</b>
				Date: Thursday, January 05, 2012 13:02:43	Rev 0

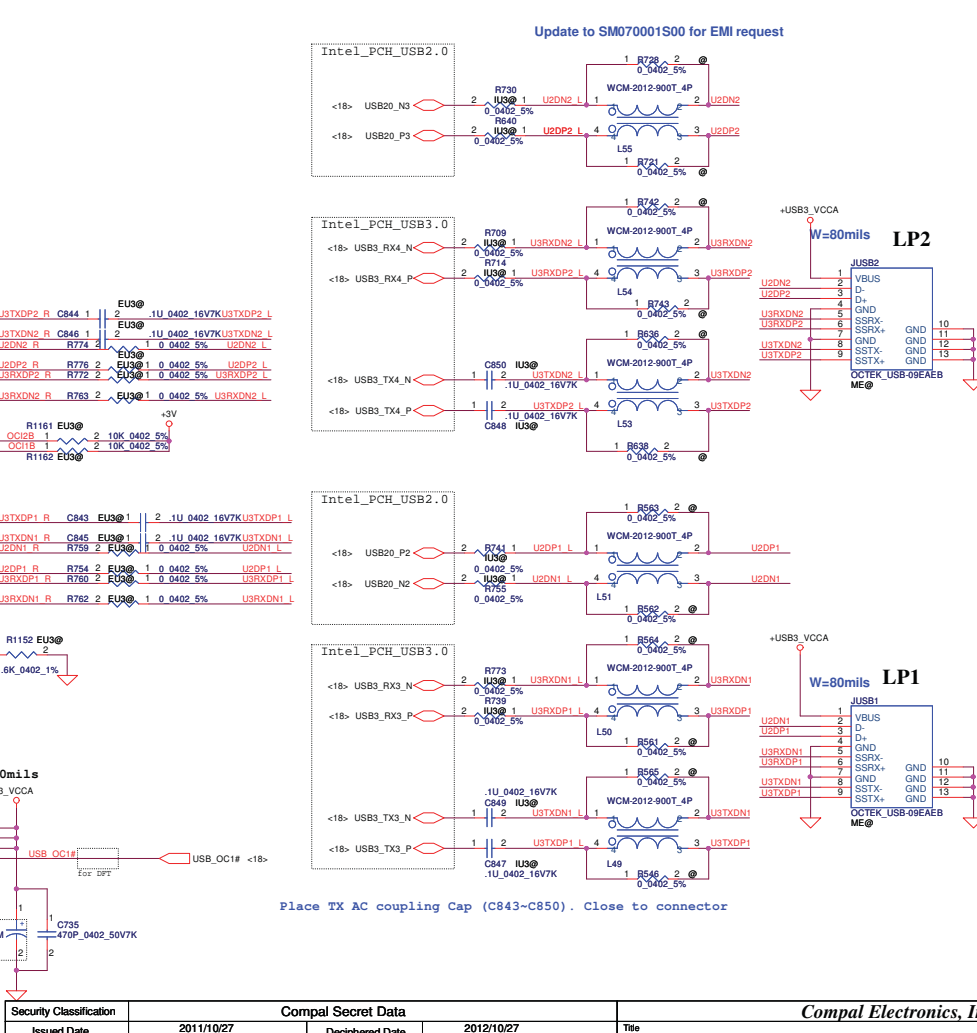
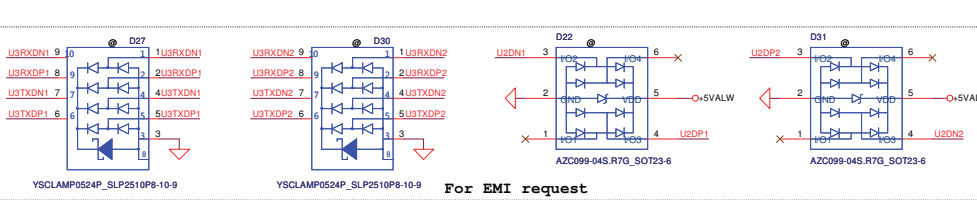
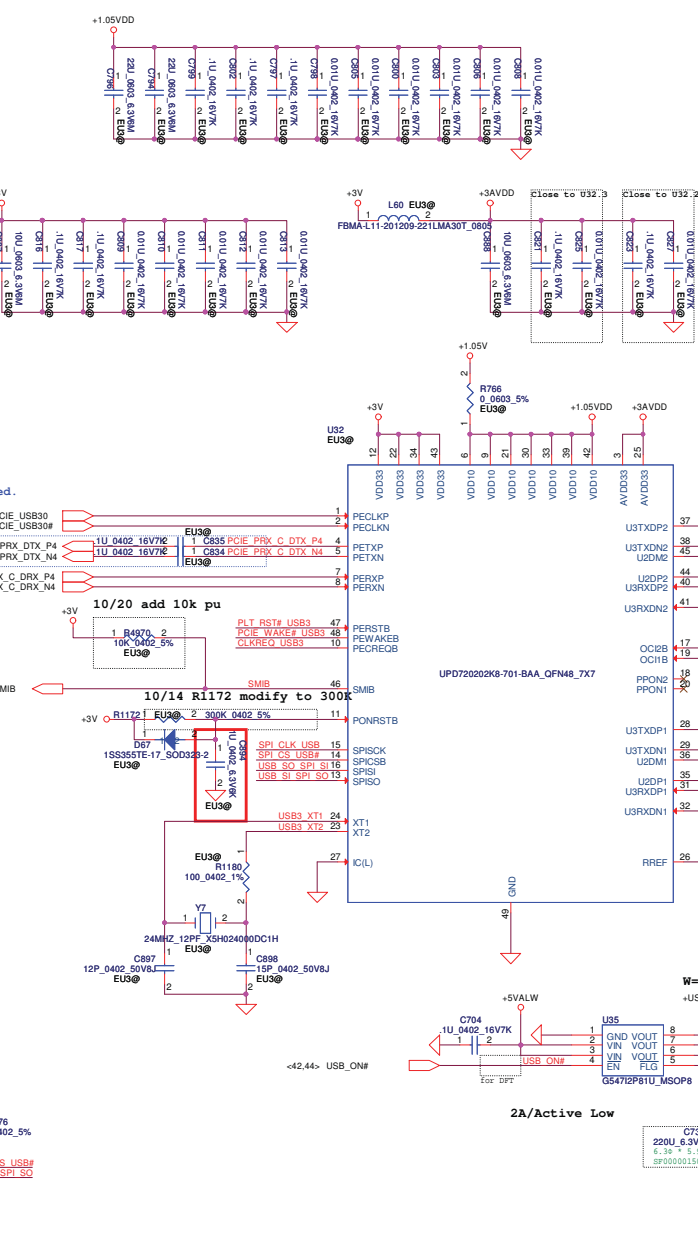
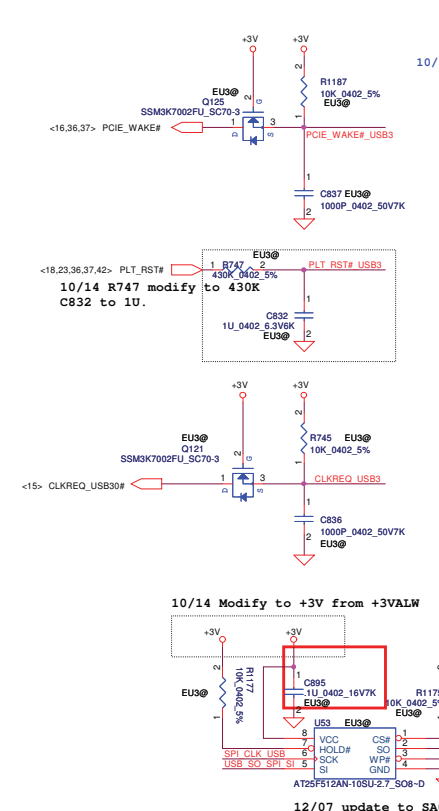
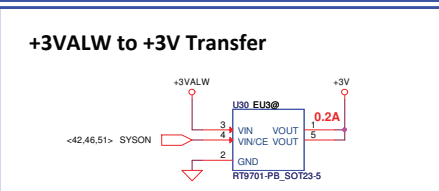
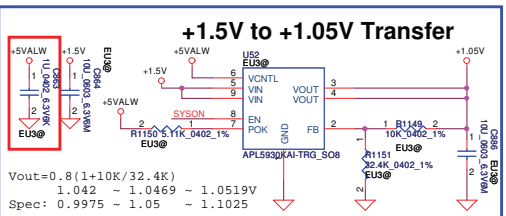
Left Ext.USB Conn.



Right Ext.USB Cable Conn.



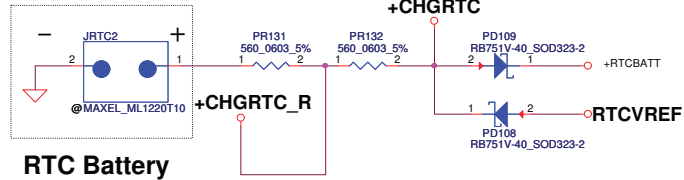
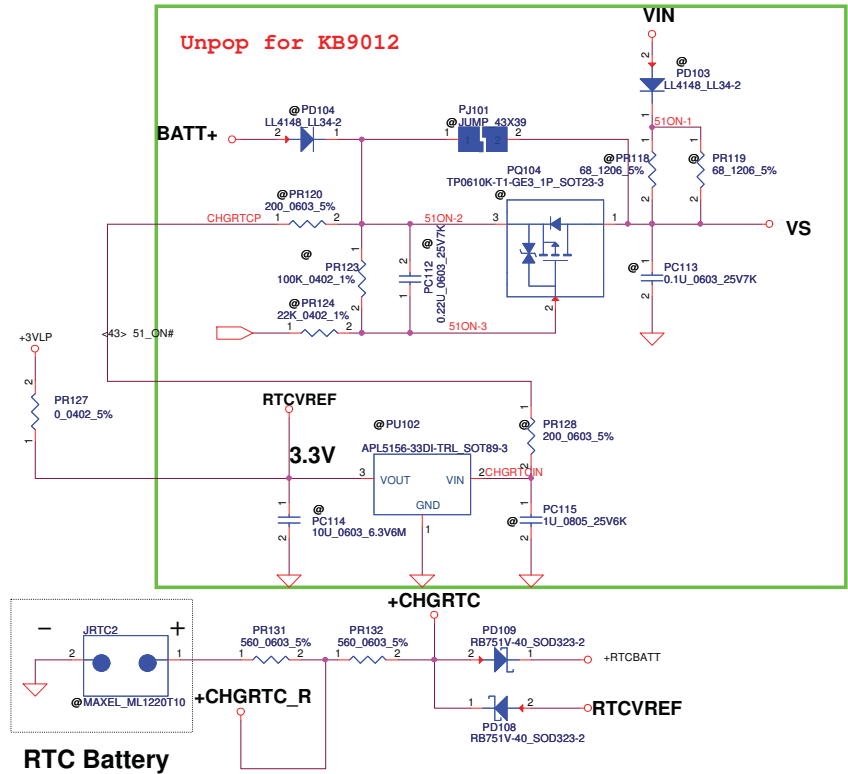
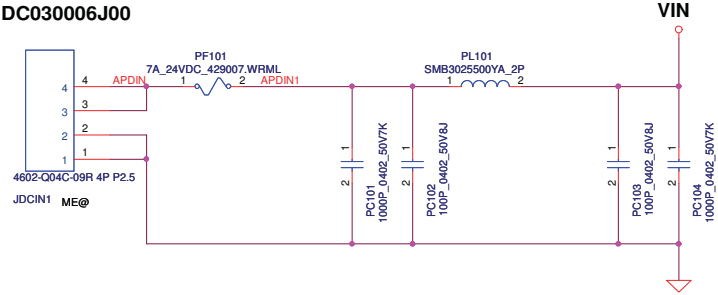
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date: Thursday, January 05, 2012	Sheet 44 of 60



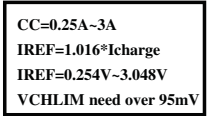
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	USB3.0/Left USB Ports
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 0.3
Size	Custom	Document Number		Date	Thursday, January 05, 2012
Sheet	45	of	60		



DC030006J00

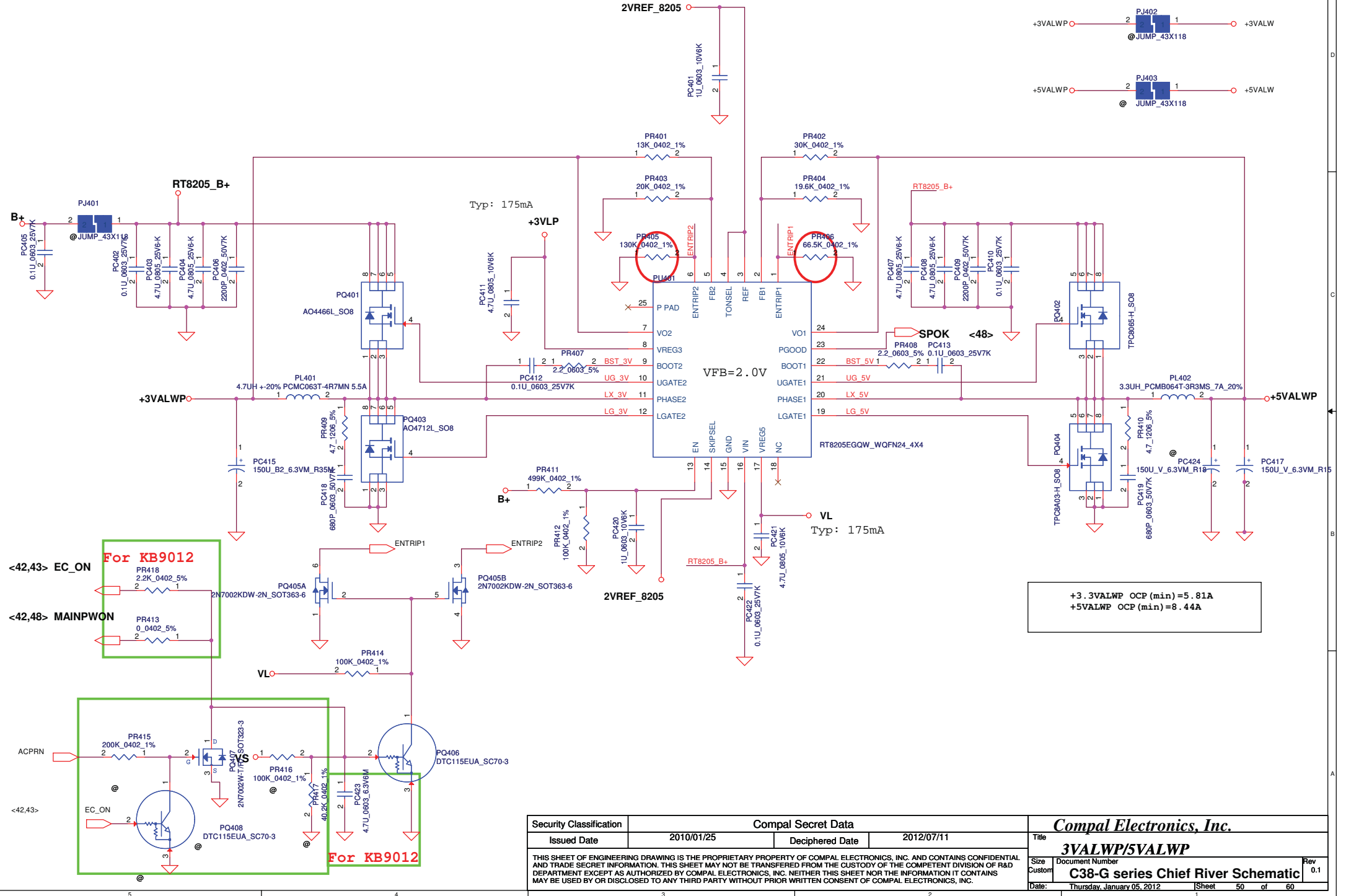




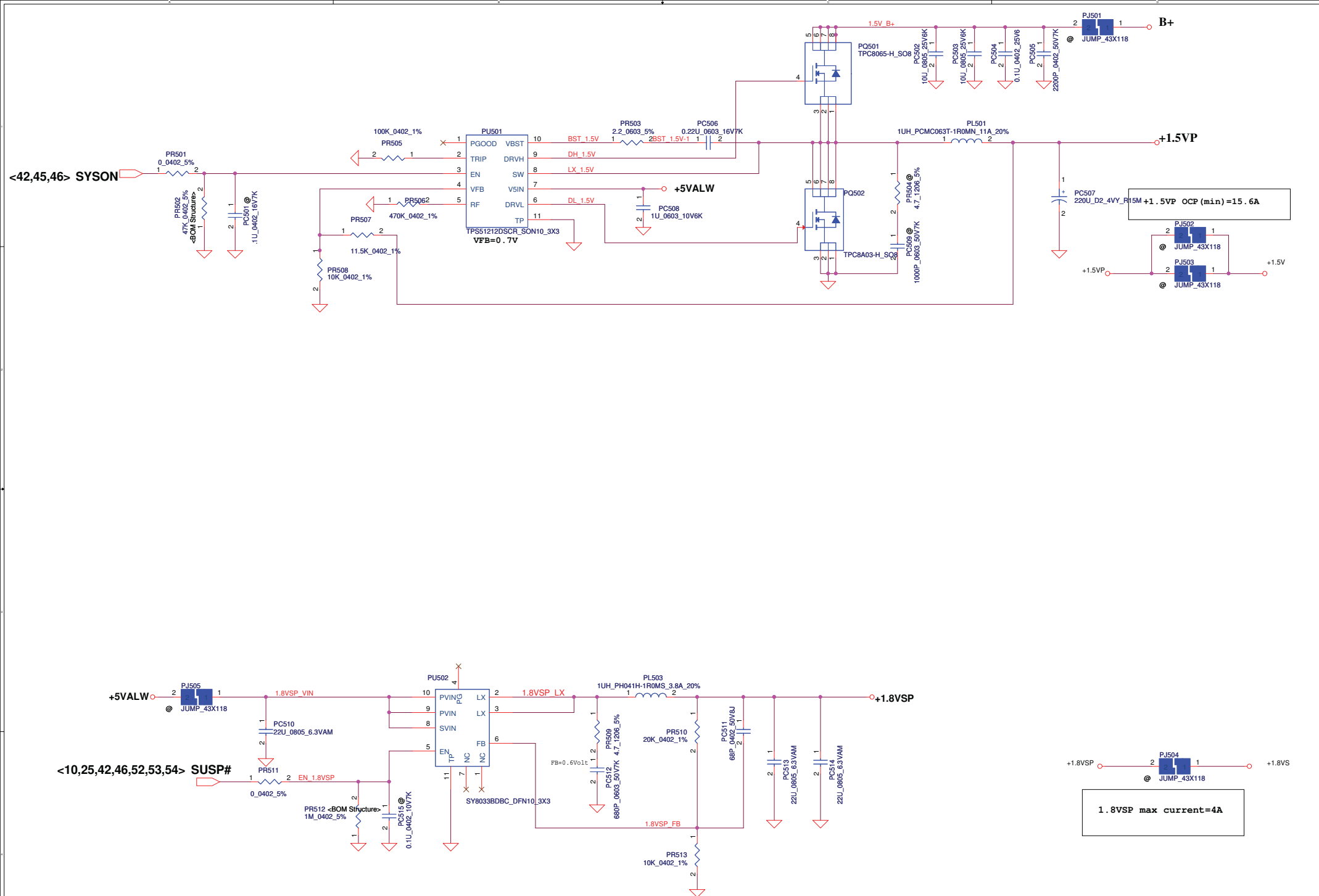


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/01/13	Deciphered Date	2012/07/11	Title	CHARGER	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 0.1
				C38-G series Chief River Schematic		
				Date:	Thursday, January 05, 2012	Sheet

Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO



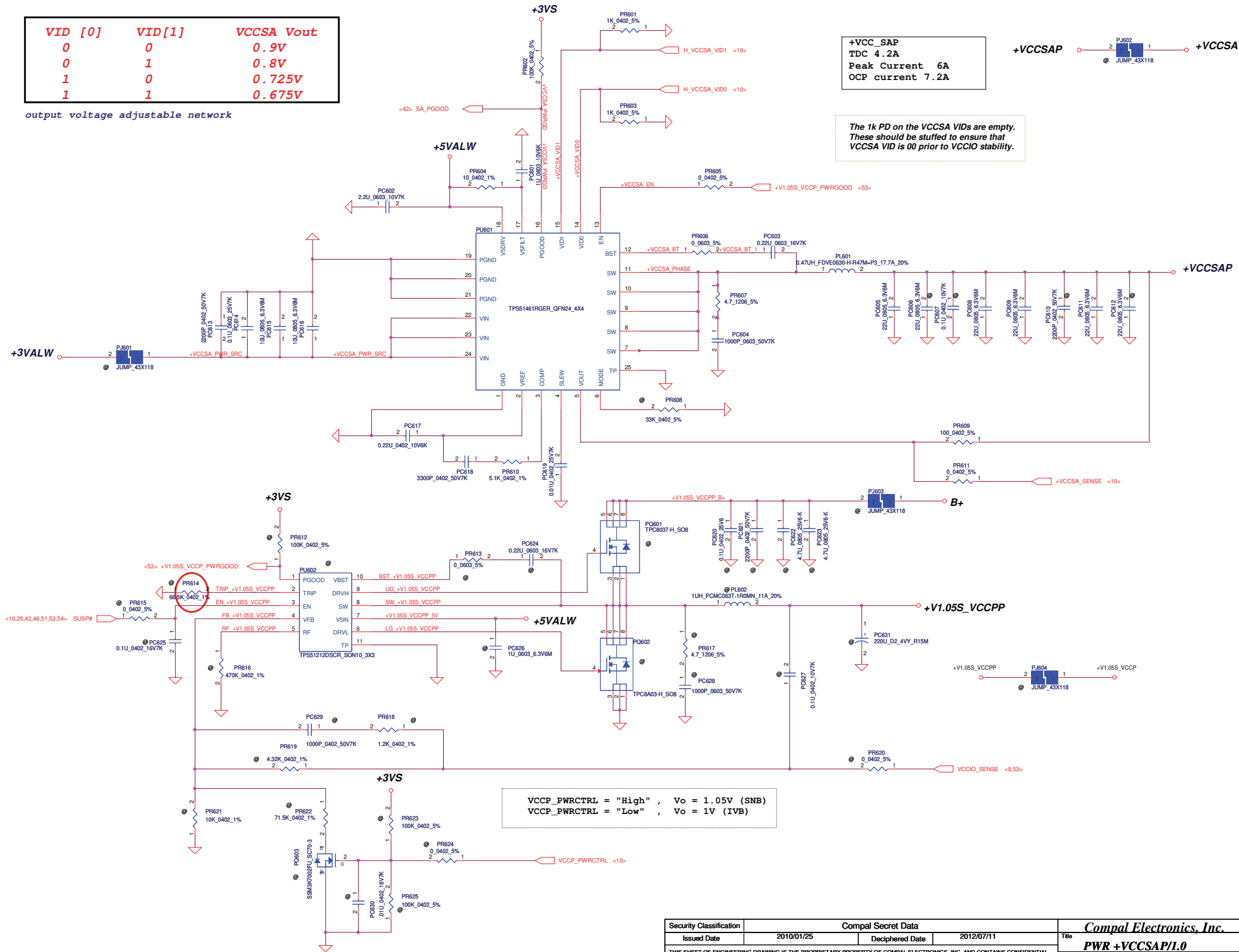
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	3VALWP/5VALWP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number C38-G series Chief River Schematic
				Date: Thursday, January 05, 2012	Rev 0.1
				Sheet 50	of 60



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR-+1.5VP/+1.8VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	C38-G series Chief River Schematic
				Date	Thursday, January 05, 2012
				Sheet	51 of 60
				Rev	0.1

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

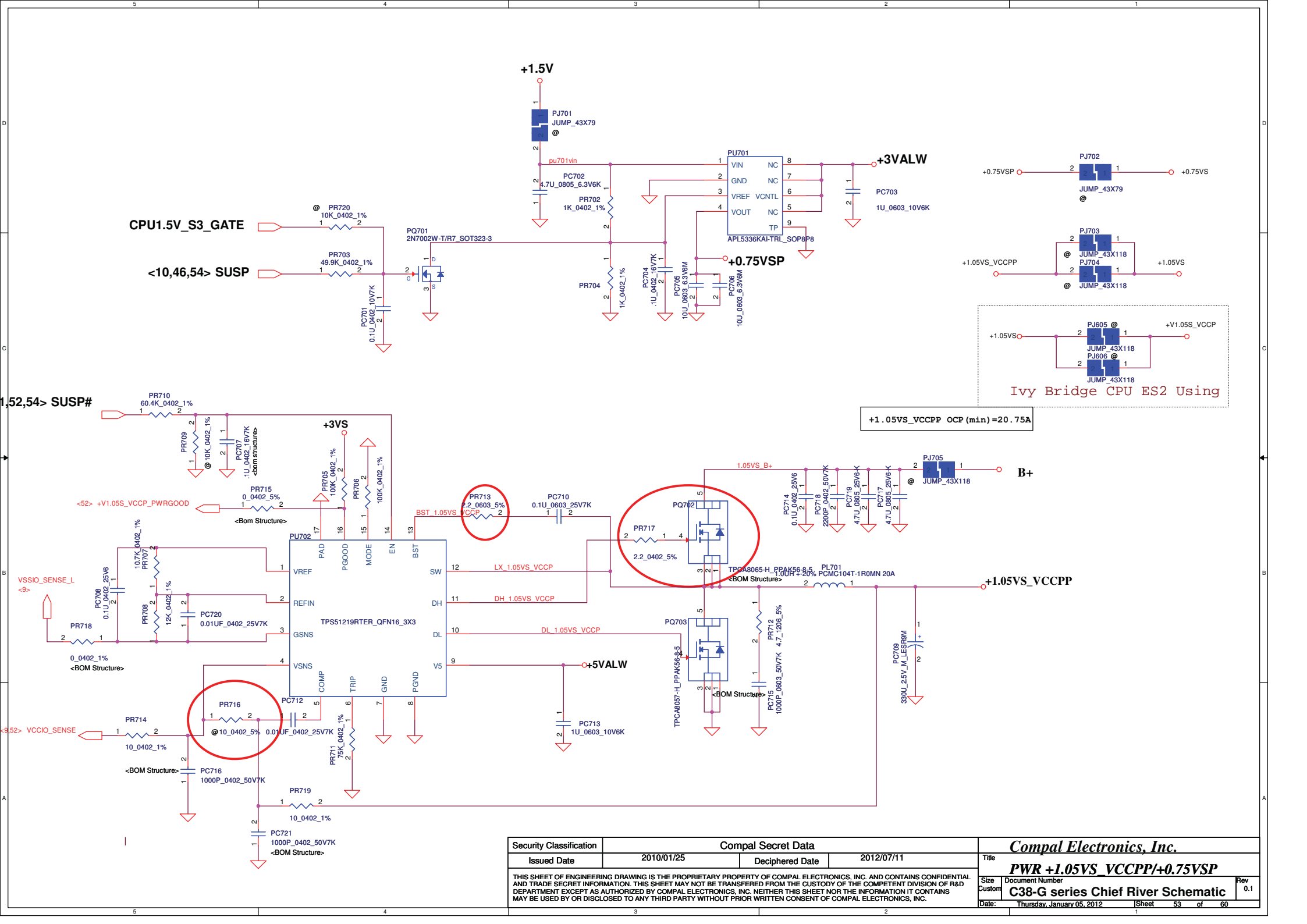
output voltage adjustable network

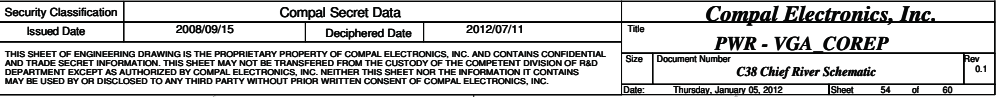


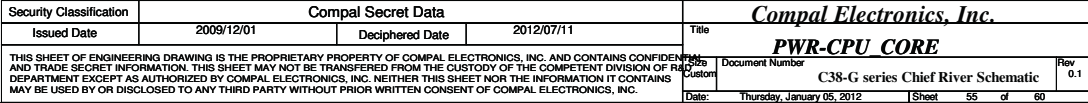
+VCCSAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

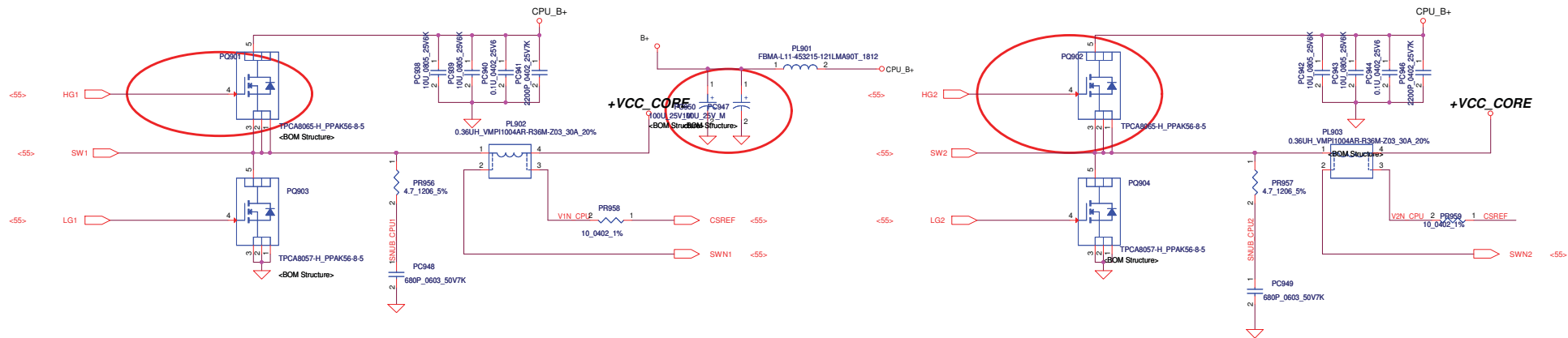
The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.

VCCP\_PWRCTRL = "High" , Vo = 1.05V (SNB)  
VCCP\_PWRCTRL = "Low" , Vo = 1V (IVB)



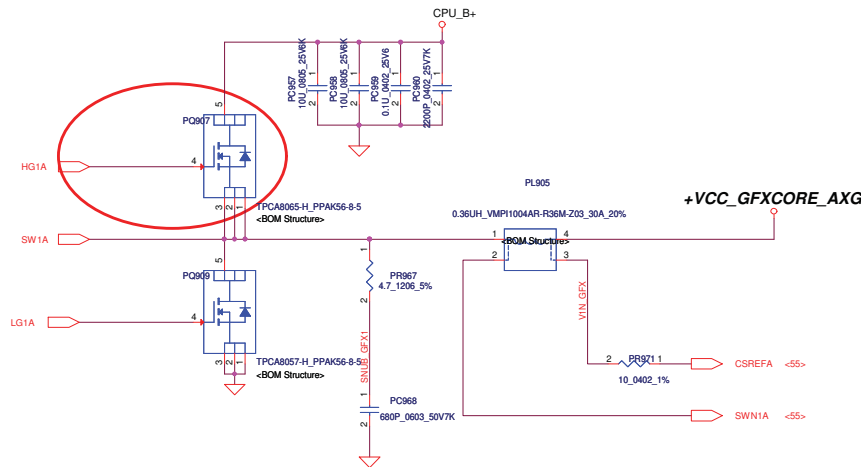






QC 45W CPU  
VID1=0.9V  
IccMax=94A  
Icc\_Dyn=66A  
Icc\_TDC=52A  
R\_LL=1.9m ohm  
OCP-110A

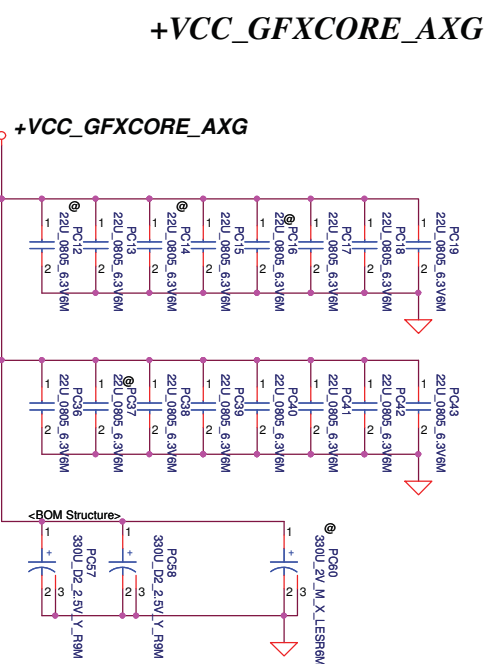
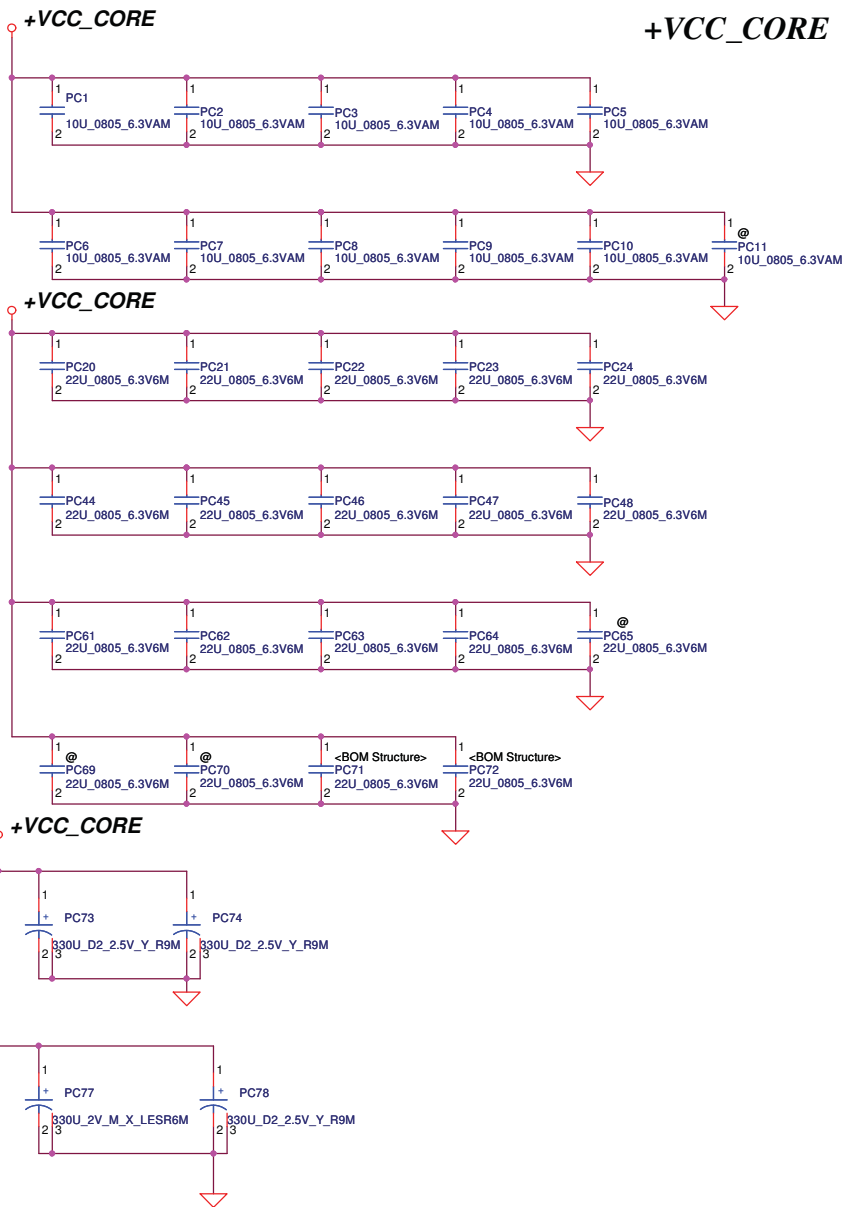
DC 35W CPU  
VID1=1.05V  
IccMax=53A  
Icc\_Dyn=43A  
Icc\_TDC=36A  
R\_LL=1.9m ohm  
OCP-65A



QC 45W GT2  
VID1=1.23V  
IccMax=46A  
Icc\_Dyn=37A  
Icc\_TDC=38A  
R\_LL=3.9m ohm  
OCP-55A

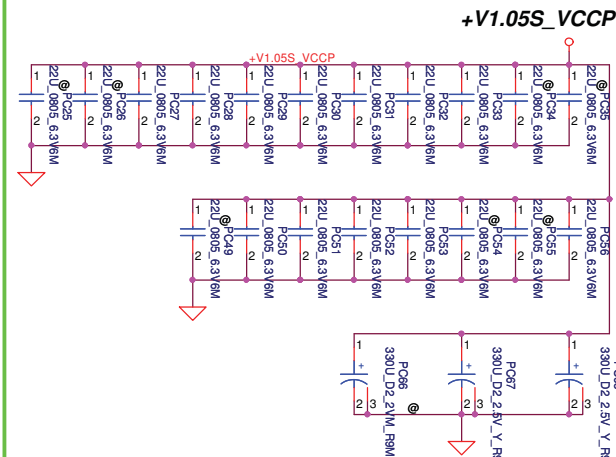
DC 35W GT2  
VID1=1.23V  
IccMax=33A  
Icc\_Dyn=20.2A  
Icc\_TDC=21.5A  
R\_LL=3.9m ohm  
OCP-40A

Security Classification		Compal Secret Data		Title	
Issued Date	2009/12/01	Deciphered Date	2012/07/11	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				C38-G series Chief River Schematic	
Date: Thursday, January 05, 2012				Sheet	56 of 60



Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

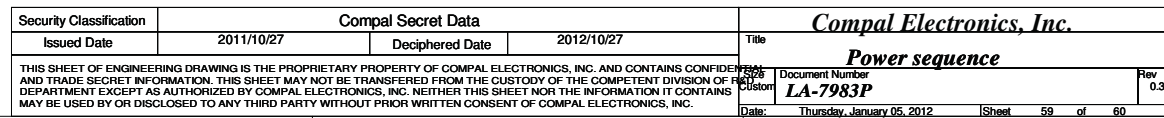


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/09/15	Deciphered Date	2012/07/11	Title	<b>PWR - PROCESSOR DECOUPLING</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number <b>C38-G series Chief River Schematic</b>	Rev 0.1
Date:	Thursday, January 05, 2012	Sheet	57	of	60	

Item	Reason for change	PG#	Modify List	Date	Phase
1	To facilitate EA test	P54	Change net name of pin 1 of PR825 from +VGA_CORE to +VGA_COREP	2011/10/19	DVT
2	Sense VSSIO_SENSE_L net close to IC	P53	Add PR718	2011/10/19	DVT
3	CPU controller compensation RC tuning	P55	Change PC904, PC907, PC908, PC909, PC926, PC928, PR929, PC936 and PR943	2011/10/19	DVT
4	EMI request	P51	Change PR503	2011/10/19	DVT
5	Back to Back MOS change	P49	Change PQ302	2011/12/06	PVT
6	Sense VSSIO_SENSE_L change according to FAE	P53	Add PR719 and PC721. Change PR718 and PR714	2011/12/06	PVT
7	Add IC G718	P48	Change PR205 to 4.42k (90W) and PR210 to 27.4k (90W)	2011/12/06	PVT
8	EC_ON RC change	P50	Change PR418 from 10k to 2.2k	2011/12/06	PVT
9	Unpop PR224 and add PR231 by HW request	P48	Unpop PR224 and add PR231	2011/12/21	PVT
10	Change CPU&GFX compensation RC by FAE recommendation	P55	PR902, PR903, PR947, PR948, PC901, PC905, PC929, PC930 and PC933	2011/12/21	PVT
11	Change charger's choke from 4.7u to 10u	P49	PL302	2011/12/21	PVT
12					
13					
14					
15					
16					
17					

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/06	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	C38-G series Chief River Schematic
Date: Thursday, January 05, 2012				Sheet	58 of 60

**MODEL NAME:** *Power Sequence Block Diagram*  
**PCB NAME:** *LA-7981P*  
**REVISION:**   
**DATE:** *2011/07/13*



## Version change list (P.I.R. List)

Page 1 of 1  
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For NVIDIA update Strapping setting.	32	RV102 change to 10K ohm	10/11	B
2	PCIE BUS corrected for external USBcontroller	45	PCIE_PRX_DTX_P4/N4 Swapped	10/11	B
3	Modify USB3.0 Controller circuit	45	R1172 to 300k, R747 to 430k, C832 to 1U	10/14	B
4	Modify USB3.0 Controller circuit	45	U53.8 to +3V, R1177.2 to +3V . Add R4970	10/14	B
5	Modify LAN function design for surge.	38	Add R4966, R4967, R4968, R4969, for 10/100 SKU	10/18	B
6		38	Modify R1443 near to LAN chip side. Delete R1448 0 ohm.	10/18	B
7		38	Modify R1443 near to LAN chip side.	10/18	B
8		38	Add CHASSIS_GND, C989, C990, C991	10/18	B
9		38	Delete R1374, R1375, R1377, DL2~DL4.	10/25	B
10	Reserve HDMI EMI solution	35	Add C992~C999	10/25	B
11	Reserve LAN ESD solution	38	Add D74, link both MCT0_1 and chassis to ground.	10/27	B
12	Change component type.	43	C987 change to 0402 type	10/27	B
13		34	C538 change to 0402 type	10/27	B
14	Reserve LAN EMI solution	38	Add R4971~R4974	10/27	B
15	Reserve MAINPWON 0ohm.	38	Add R4978	12/21	C
16	LAN Power Switch	37	Add Q130, R4977, C1001	12/21	C
17					

Security Classification	Compal Secret Data			Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
Date: Thursday, January 05, 2012				Sheet	60 of 60